TITLE ：NV105WAM-N31

Customer: Solar

Product Specification

Rev. 0

BOE Optoelectronics Technology Co., Ltd

REVISION HISTORY

(√)Preliminary Specification

( )Final Specification

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P0	64	Initial Release	2019.05.30	Gao Shaohong
P1	64	Page 12/36/37	2019.06.14	Gao Shaohong
P2	64	Page 12/33/35/36/37	2019.08.13	Gao Shaohong
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0	64	Page 5/7/11/12/31/33/42	2019.12.10	Gao Shaohong

REVIEWED	
Designer	**Manager**
Xu Zhuo(Array)	Ma Xiaofeng
Yang Haigang(Cell)	Ma Xiaofeng
Liu Chao(CF)	Li Min
Chen Shuai(EE)	Ma Xiaofeng
Fu Jie(MO)	Ma Xiaofeng
Luo Jinliang(QE)	Cui Chaoyang
Wen Jianghong(PI)	Chen Gang
APPROVED	
Gao shaohong(PM)	

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

NV105WAM-N31 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 10.51 inch diagonally measured active area with Full-HD+ resolutions (1920 horizontal by 1280 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M(8bit) colors and color gamut sRGB100%. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. All input signals are eDP1.4a interface compatible.

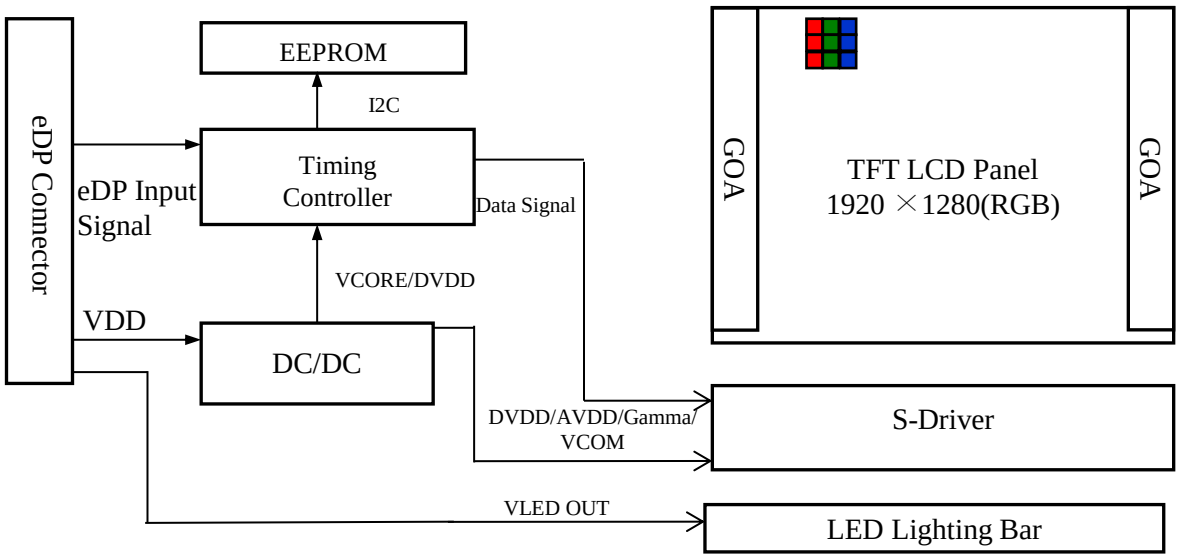


Figure 1. Drive Architecture

1.2 Features

- 2 lane eDP interface with 2.7Gbps link rates
- Thin and light weight
- 16.7M (8bit) color depth, color gamut SRGB 100%
- Single LED lighting bar (Bottom side/Horizontal Direction)
- Data enable signal mode
- Green product (RoHS & Halogen free product)
- Low driving voltage and low power consumption
- On board EDID chip
- DPCD Version 1.2
- Function：PSR2+LRR/BIST/Instant on

1.3 Application

- Notebook PC (Wide type)

1.4 General Specification

The followings are general specifications at the model NV105WAM-N31. (listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	222.048(H) ×148.032 (V)	mm	
Number of pixels	1920 (H) ×1280 (V)	pixels	
Pixel pitch	115.65(H) ×115.65 (V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(8bit)		
Color gamut	TYP:sRGB 100%, Min:sRGB:96%.		
Display mode	Normally black		
Dimensional outline	227.048±0.4 (H)*157.732±0.4(V)(W/ FPC bending)*1.95 (Max)(W/O PCB) 227.048±0.4 (H)*157.732±0.4(V)(W/ FPC bending)*4.5 (Max)(W/ PCB)	mm	
Weight	115(max)	g	
Surface treatment	HC		
Surface hardness	2H		
Back-light	Bottom edge side, 1-LED lighting bar type		Note 1
Power consumption	P_D : 0.42(Max)	W	@60HZ @Mosaic
	P_{BL} : 1.69(Max)	W	
	P_{Total} : 2.08(Max)	W	@Mosaic

Notes : 1. LED Lighting Bar (45*LED Array)

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.

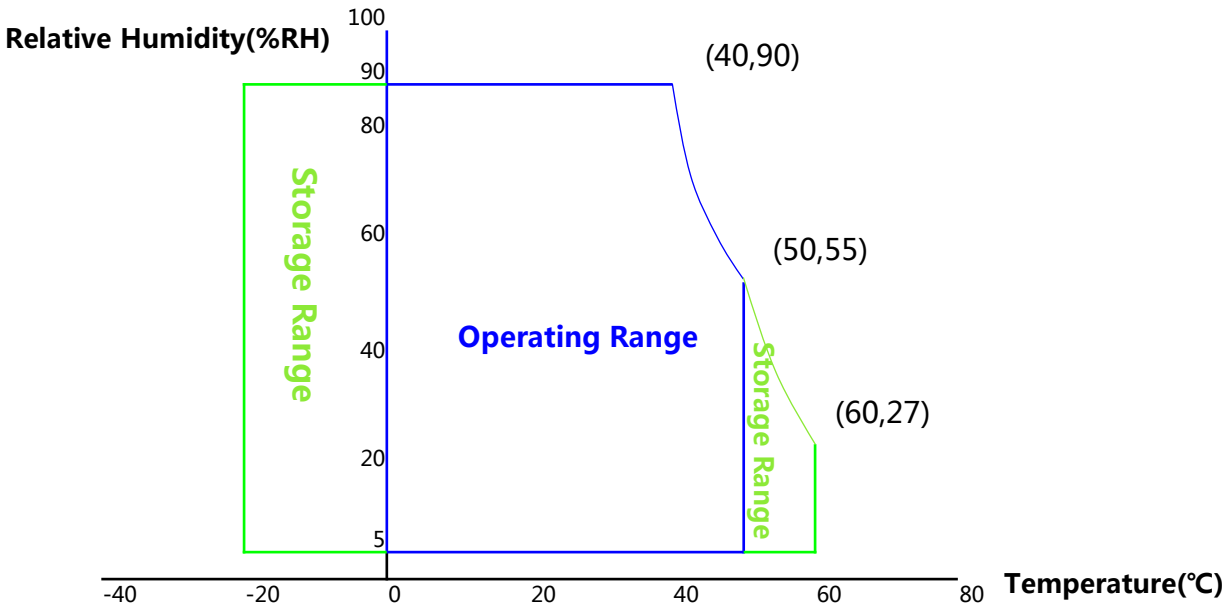


Figure 2. Temperature and Relative Humidity Range

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage		V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage		V_{RF}	-10% VDD	-	+10% VDD	V	@ V_{DD} = 3.3V
Power Supply Inrush Current		Inrush	-	-	2	A	Note3
Power Supply Current	Mosaic	I_{DD}	-	-	136	mA	Note 1
	RGB		-	-	136	mA	
	Solid		-	-	267	mA	
Power Consumption	Mosaic	P_M	-	0.36	0.42	W	
	RGB	P_{RGB}	-	0.36	0.42	W	
	Solid	P_S	-	-	0.71	W	
	BLU	P_{BL}	-	-	1.69	W	Note 2
	Total	P_{Total}	-	-	-	W	@Mosaic

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

Notes :

1. The supply voltage is measured and specified at the interface connector of LCM.
   The current draw and power consumption specified is for 3.3V at 25 ˚C.
   a) Mosaic pattern 8*8
   b) R/G/B patterns
   c)Solid pattern(maximum logic power consumption) : Skip sub pixel

(a) (b) (c)

Figure 3. Power Measure Patterns

2. Calculated value for reference ($V_{LED} \times I_{LED}$)
3. Measure condition (Figure 4)

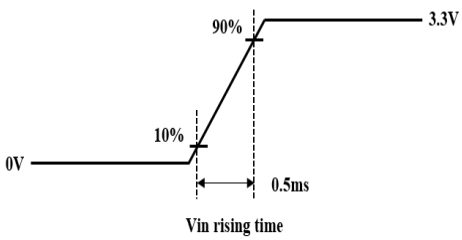


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2˚C

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage	V_F	-	-	2.9	V	
LED Forward Current	I_F	-	12.4	-	mA	
LED Life-Time	N/A	15,000	-	-	Hour	I_F = 12.4mA Note 2

3.3 LED Structure

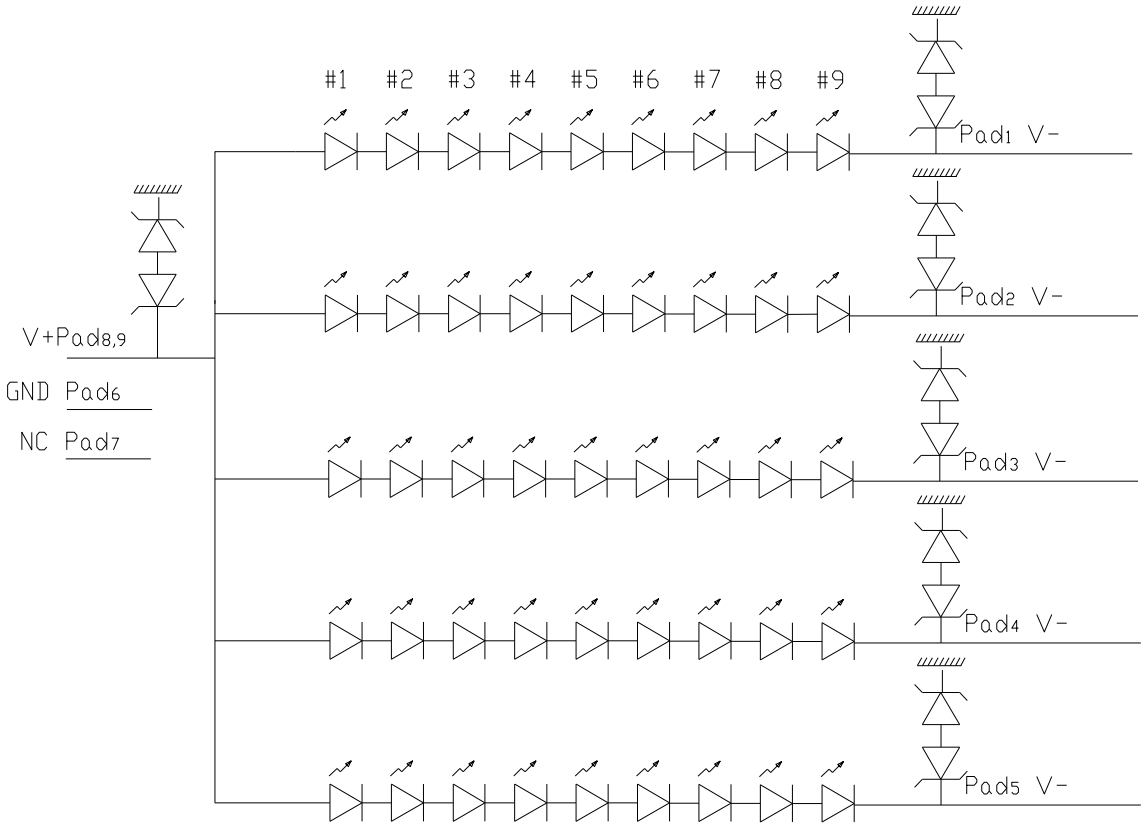


Figure 5. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (PR730&PR810) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol		Condition		Min.	Typ.	Max.	Unit	Remark
Uniformity	Luminance(13P)	-		Θ = 0°		70	-	-	%	Note 1
	Color(13P)	R/G/B/W	Δu'			-	-	0.01		
			Δv'			-	-	0.013		
			Δu'v'			-	-	0.013		
Contrast Ratio	5 Points	CR		Θ = 0°		1000	1500	-		Note 2
Contrast performance				Θ=20	Φ=0/90/180/270	45	45		%	Note 3
				Θ=40	Φ=0/90/180/270	20	25			
				Θ=60	Φ=0/90/180/270	10	15			
				Θ=85	Φ=0/90/180/270	3	3			
Luminance	5 Points	Y_w		Θ = 0° ILED = 12.4mA		320	420	-	cd/m^2	Note 4
Luminance Performance	5 Points	-		Θ=20	Φ=0/90/180/270	55	60	-	%	
		-		Θ=40	Φ=0/90/180/270	15	20			
		-		Θ=60	Φ=0/90/180/270	10	15			
FWHM	Horizontal	-		Luminance decrease≤1/2		20	30			
	Vertical	-				20	30			
Transmittance		Tr.		Θ = 0°		6.8	7.60		%	
Reflectance	Specular	-				-	5.85	-		
	Diffuse	-				-	5.87	-		

<Table 5. Optical Specifications>

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
White Chromaticity		W_x	Θ = 0°		0.288	0.313	0.338		Note 5
		W_y			0.304	0.329	0.354		
Reproduction of Color	Red	R_x	Θ = 0°		Typ.-0.025	0.646	Typ.+0.025		
		R_y				0.329			
	Green	G_x				0.300			
		G_y				0.612			
	Blue	B_x				0.152			
		B_y				0.063			
	Black	Dx				0.265			For reference
		Dy				0.254			
Color Gamut					96	100	-	%	sRGB Matching Rate
R/G/B/W color performance		△u'v'	Θ=20	Φ=0/90/180/270	-	-	0.01		
		△u'v'	Θ=40	Φ=0/90/180/270	-	-	0.02		
		△u'v'	Θ=60	Φ=0/90/180/270	-	-	0.025		
Black color performance		△u'v'	Θ=20	Φ=0/90/180/270	-	-	0.03		
		△u'v'	Θ=40	Φ=0/90/180/270	-	-	0.03		
		△u'v'	Θ=60	Φ=0/90/180/270	-	-	0.03		
Luminance-% of R,G,B		L-%(R) = L(R) / L(W)	Θ = 0°		Typ.-1%	22.1%	Typ.+1%		
		L-%(G) = L(G) / L(W)			Typ.-2%	70.6%	Typ.+2%		
		L-%(B) = L(B) / L(W)			Typ.-0.5%	7.3%	Typ.+0.5%		
Gamma			Θ = 0°		2.0	2.2	2.4		
Angular gamma			Θ=20	Φ=0/90/180/270	1.9	2.2	2.5		
			Θ=40	Φ=0/90/180/270	1.9	2.2	2.5		
			Θ=60	Φ=0/90/180/270	1.8	2.2	2.6		
Response Time (Rising + Falling)	Black to white	T_{RT}	Ta= 25℃ Θ = 0°		-	-	30	ms	Note 6
	Gray to Gray	GTG			-	-	50	ms	
Image sticking		Rw	Ta= 25℃ Θ = 0°				1.017		Note 7
		Rb					1.135		
Flicker	Center	dB	Ta= 25℃ Θ = 0°				-30		Note 8
	Non-center						-25		
Cross Talk		CT	Θ = 0°		-	-	2.0	%	Note 9

Notes :

1. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 13 points / Maximum Luminance of 13 points.(see Figure 8).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The figure 9 shows a polar coordinate system to define viewing angles or measurement angles relative to the surface of a display. Customarily, the "top" side of the display corresponds to the "12 o'clock" viewing direction (φ= 90◦), and other viewing directions are similarly related to positions of the hour hand on a clock. The sub-pixel drawn is to illustrate the orientation of the display active area

4. Center Luminance of white is defined as luminance values of 5 point average(4,5,7,9,10) across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Tf. The GTG measurements are to be taken on all of the combinations(0/31/63/95/127/159/191/223/255).

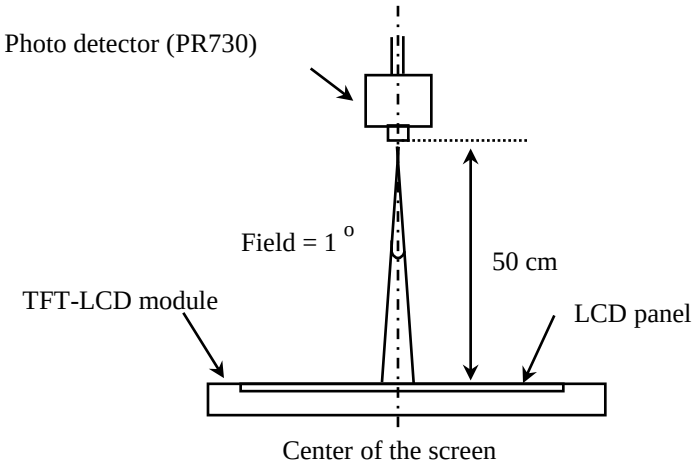
7. Set the LCD display to show a 100% Black / 100% White 5x5 checkerboard pattern for 24 hours at display maximum luminance at room temperature. After the 24 hours, set the LCD display to show a full screen white (255 Gray) and black (0 Gray) and report white and black residual image factor of Rw and Rb, respectively (see Figure 11)

$$R_W = \frac{\max[(K_{WR}+K_{WL})L_{WC},(L_{WL}+L_{WR})K_{WC}]}{\min[(K_{WR}+K_{WL})L_{WC},(L_{WL}+L_{WR})K_{WC}]},\quad R_B = \frac{\max[(K_{BR}+K_{BL})L_{BC},(L_{BL}+L_{BR})K_{BC}]}{\min[(K_{BR}+K_{BL})L_{BC},(L_{BL}+L_{BR})K_{BC}]}$$

8.Flicker test takes the JEITA measurement method. Measurements should be done at 60Hz, 48Hz, and other low refresh in a dark room (<1 Lux ambient lighting.).Load the relevant (worst case) flicker pattern for panel with luminance level 255.Measure the flicker level of 13 points .

9. The grays are 186 gray level and 0 gray level. In each case, the luminance measurements are to be taken while the respective test patterns are displayed. (See Figure 12).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 6. Measurement Set Up

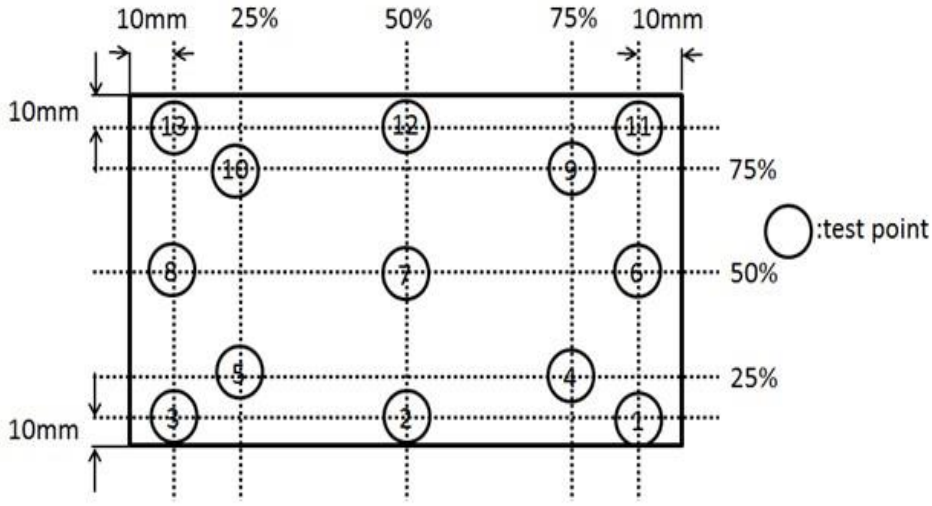


Figure 7. White Luminance and Uniformity Measurement Locations (13 points)

Center Luminance of white is defined as luminance values of center 7 point across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

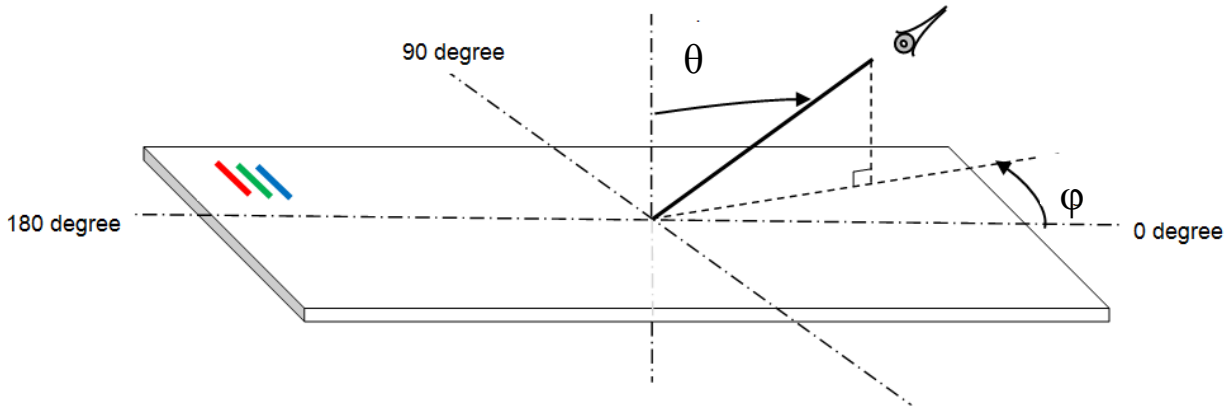


Figure 8. Definition of Axis

The White luminance uniformity on LCD surface is then expressed as : ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 8).

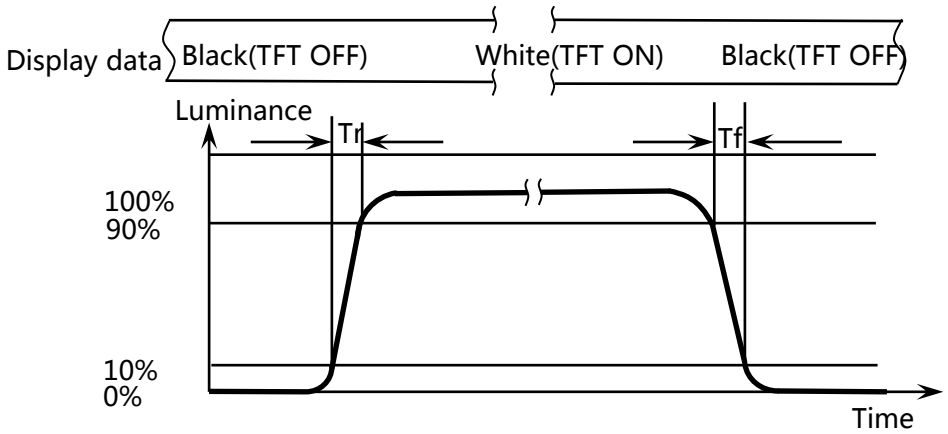


Figure 9. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : LMS PR810

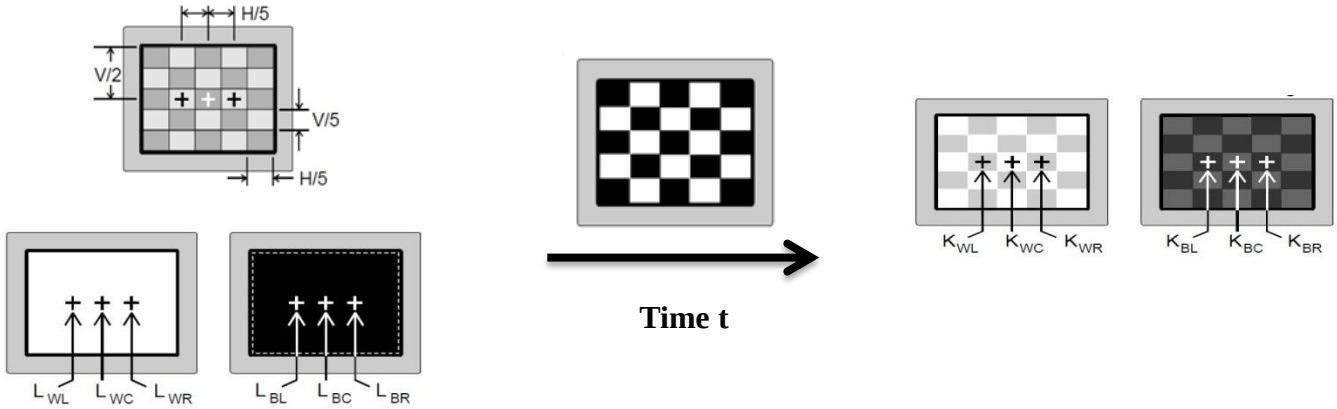
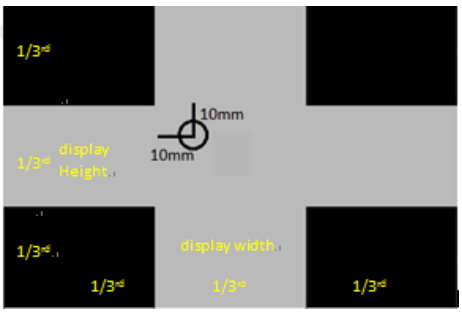
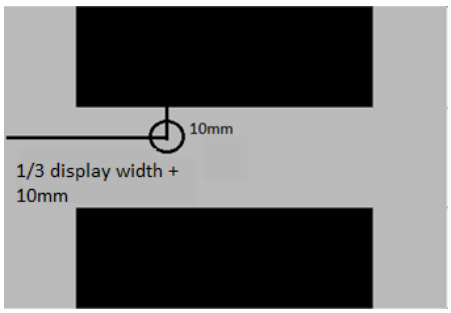


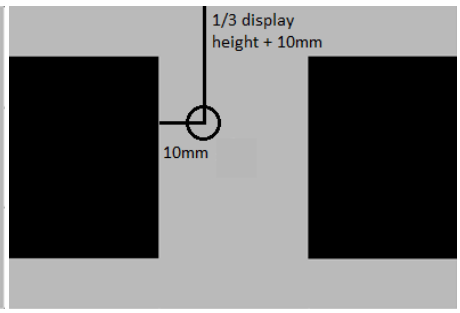
Figure 10. Cross Talk Modulation Test Description



Display Pattern for Lref



Display pattern for Lver



Display Pattern for Lh

$$\text{Vertical Crosstalk} = (|L_{ver}-L_{ref}|/L_{ref})*100\%$$

$$\text{Horizontal Crosstalk} = (|L_{h}-L_{ref}|/L_{ref})*100\%$$

Figure 11. Cross Talk Modulation Test Description

The test system: PR730

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is AXE550127
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

PIN NO	Symbol Function	Description	PIN NO	Symbol Function	Description
1	VCC3.3	LCD logic and driver power	2	VCC3.3	LCD logic and driver power
3	VCC3.3	LCD logic and driver power	4	NC	NC
5	NC	NC	6	instant on	TCON Support funticon
7	GND	LCD logic and driver ground	8	GND	LCD logic and driver ground
9	GND	LCD logic and driver ground	10	H_GND	High Speed Ground
11	EDP_TXN0	Comp Signal Link Lane 0	12	NC	NC
13	EDP_TXP0	True Signal Link Lane 0	14	H_GND	High Speed Ground
15	H_GND	High Speed Ground	16	H_GND	High Speed Ground
17	EDP_TXN1	Comp Signal Link Lane 1	18	NC	NC
19	EDP_TXP1	True Signal Link Lane 1	20	H_GND	High Speed Ground
21	H_GND	High Speed Ground	22	H_GND	High Speed Ground
23	EDP_AUXP	True Signal Auxiliary Ch.	24	NC	NC
25	EDP_AUXN	Comp Signal Auxiliary Ch.	26	H_GND	High Speed Ground
27	H_GND	High Speed Ground	28	EDP_HPD	HPD signal pin
29	LCD_Self_Test or NC	LCD Panel Self Test Enable (Optional)	30	GND	LCD logic and driver ground
31	BLKT-FB1	LED Cathode	32	BLKT-FB2	LED Cathode
33	BLKT-FB3	LED Cathode	34	BLKT-FB4	LED Cathode
35	BLKT-FB5	LED Cathode	36	NC	NC
37	NC	NC	38	VLED	LED Anode
39	VLED	LED Anode	40	VLED	LED Anode
41	NC	NC	42	NC	NC

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is AXE550127
The connector interface pin assignments are listed in Table 6.

<Table 7. Pin Assignments for the Interface Connector>

PIN NO	Symbol Function	Description	PIN NO	Symbol Function	Description
43			44		
45			46		
47			48		
49			50		

Note:
Touch pin has been deleted in DV.

5.2 eDP Interface

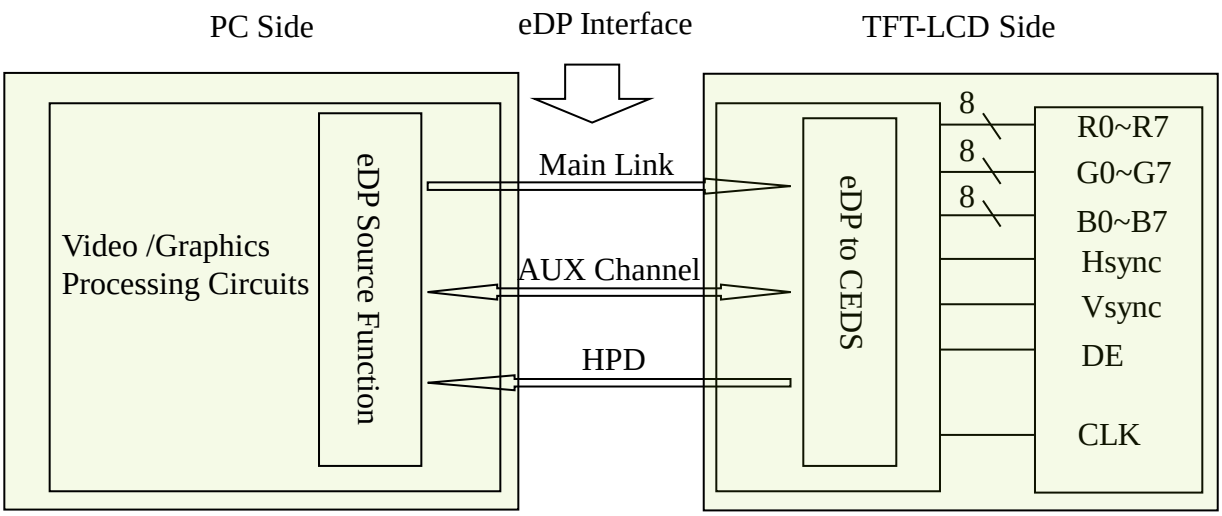


Figure 12. eDP Interface Architecture

Note:
Transmitter : Parade DP501 or equivalent.
Transmitter is not contained in module.

5.3 Data Input Format

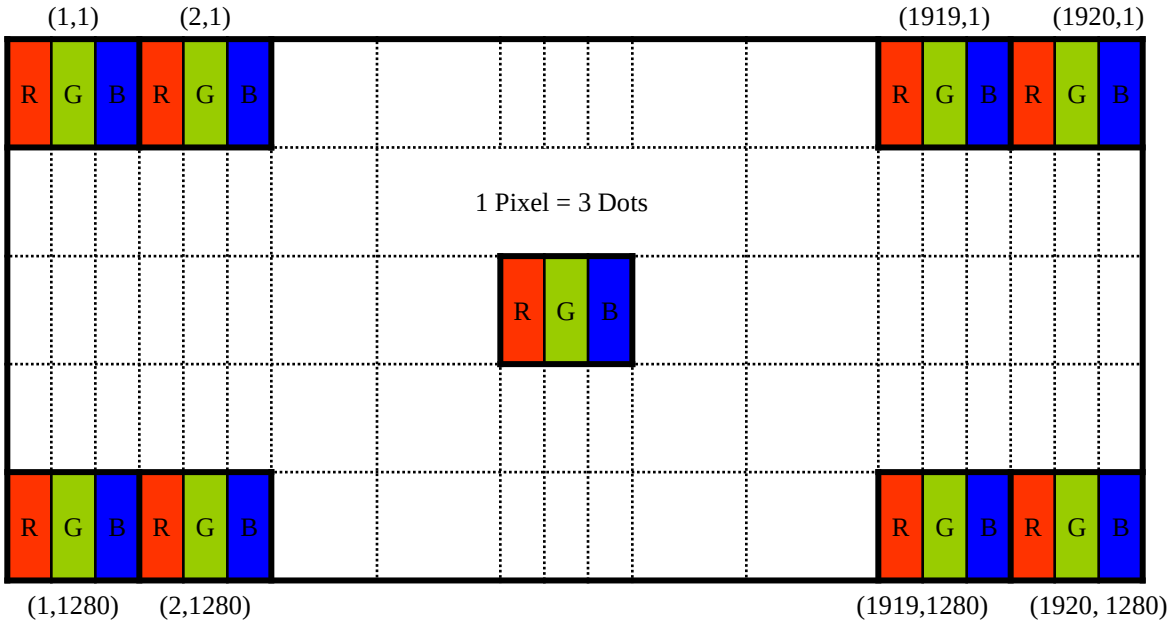


Figure 13. Display Position of Input Data (1920-1280)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector:MSAK24037P9.

<Table 8. Pin Assignments for the BLU Connector>

PIN NO	Symbol Function	Description	PIN NO	Symbol Function	Description
1	BLKT-FB1	LED Cathode	2	BLKT-FB2	LED Cathode
3	BLKT-FB3	LED Cathode	4	BLKT-FB4	LED Cathode
5	BLKT-FB5	LED Cathode	6	GND	GND
7	NC	NC	8	VLED	LED Anode
9	VLED	LED Anode			

6.0 SIGNAL TIMING SPECIFICATION

6.1 The NV105WAM-N31 Is Operated By The DE Only

< Table 9. Signal Timing Specification >

Item		Symbols	Min	Typ	Max	Unit	NOTE
Clock	Frequency	1/Tc		164.82	180	MHz	
Frame Period		Tv	1310	1340	1390	lines	Max值基于Htotal为Tpy计算，预留5%margin
			-	60	-	Hz	
			-	16.67	-	ms	
Vertical Display Period		Tvd	-	1280	-	lines	
One line Scanning Period		Th	2000	2050	2120	clocks	Max值基于Vtotal为Tpy计算，预留5%margin
Horizontal Display Period		Thd	-	1920	-	clocks	

Note : The above is as optimized setting.

6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 9.

<Table 10. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
EYE width at package pins	V_{RX-EYE}	0.6			UI	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	180	-	1380	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	100	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	50	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	60	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

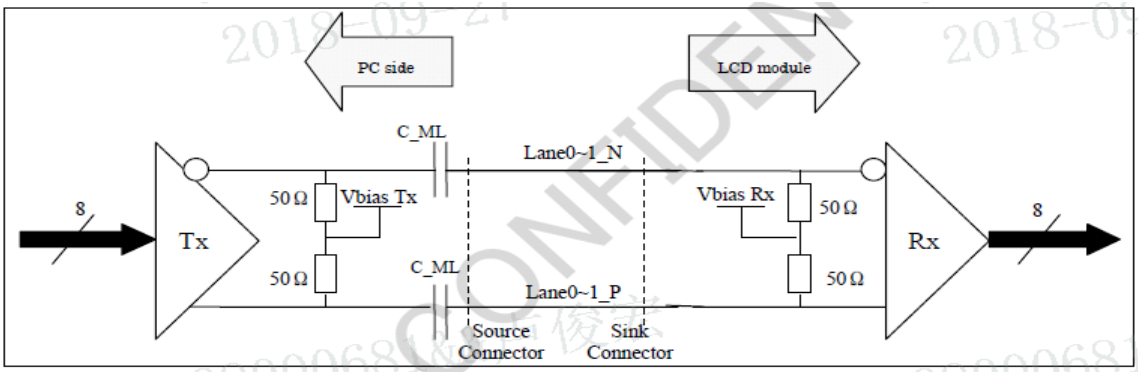


Figure 14. Main link differential pair

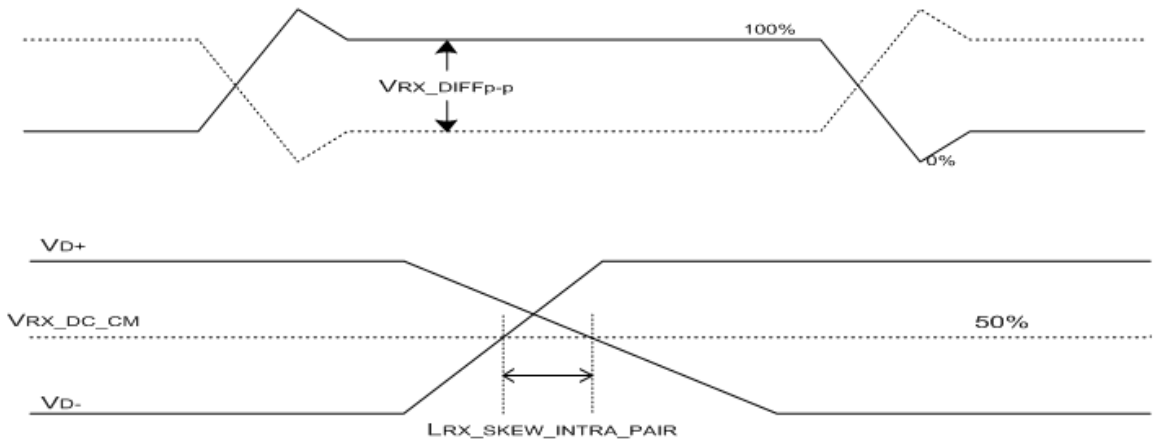


Figure 15. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

<Table 11. HPD Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
HPD voltage	V_{HPD}	2.25	-	3.6	V	
Hot Plug Detection Threshold	-	2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold	-	-	-	0.8V	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1	ms	
HPD_TimeOut	-	2.0	-	-	ms	

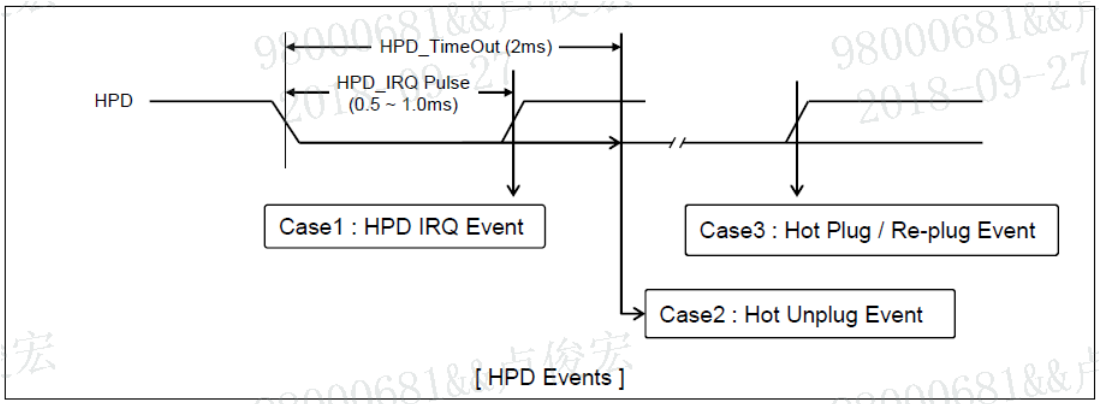


Figure 16. HPD Events

<Table 12. AUX Characteristics>

Item	Symbol	Min	Typ	Max	Unit	Remark
AUX unit interval	UIAUX	0.4	0.5	0.6	Us	
AUX peak-to-peak input differential voltage	VAUX-RX-DIFFp-p	0.29	-	1.38	V	
AUX CH termination DC resistance	RAUX-TERM	80	100	120	Ohm	
AUX DC common mode voltage	VAUX-DC-CM	0	-	2	V	
AUX turn around common mode voltage	VAUX-TURN-CM	-	-	0.3	V	
AUX short circuit current limit	IAUX-SHORT	-	-	90	mA	
AUX AC Coupling Capacitor	CSOURCE-AUX	75	-	200	nf	Source side

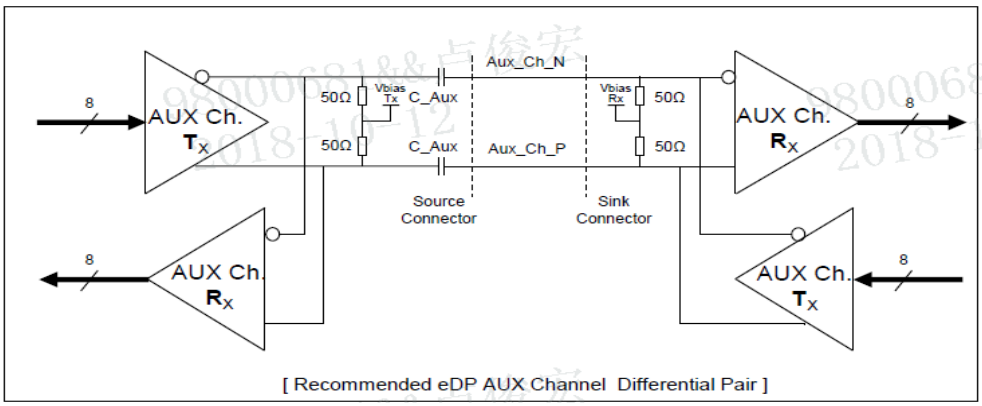


Figure 17. AUX differential pair

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 13. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																							
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ ▽					↑ ↓								↑ ↓								↑ ↓			
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△ ▽					↑ ↓								↑ ↓								↑ ↓			
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△ ▽					↑ ↓								↑ ↓								↑ ↓			
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray scale of White & Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	△ ▽					↑ ↓								↑ ↓								↑ ↓			
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
	▽	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

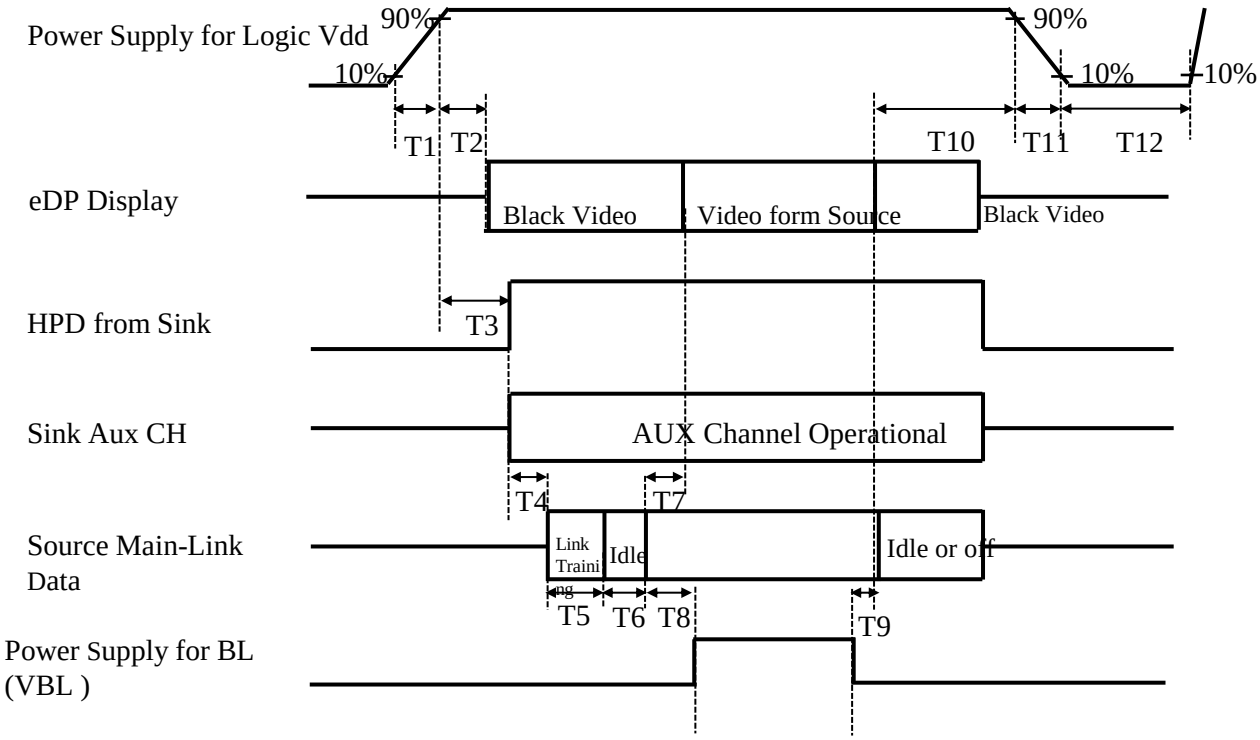


Figure 18. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 0.5ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

3.TCON POWER ON SEQUENCE refer to Appendix D.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 14.1. edp Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	PANASONIC Corporation
Type/ Part Number	AXE550127-50pin
Mating Housing/ Part Number	AXE650127-50pin

< Table 14.2. Touch Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	HRS
Type/ Part Number	FH34SRJ-8S-0.5SH(50)
Mating Housing/ Part Number	

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23shows mechanical outlines for the mode NV105WAM-N31.
Other parameters are shown in Table 14.

<Table 15. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	222.048(H) ×148.032 (V)	mm
Number of pixels	1920 (H) X 1280 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	115.65(H) ×115.65 (V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	262K(6bit)	
Display mode	Normally black	
Dimensional outline	227.048±0.4 (H)*157.732±0.4(V)(W/ FPC bending)*1.95 (Max)(W/O PCB) 227.048±0.4 (H)*157.732±0.4(V)(W/ FPC bending)*4.5 (Max)(W/ PCB)	mm
Weight	115 (max)	g

10.2 Mounting

See Figure 23.

10.3 Surface Treatment and Polarizer Hardness.

The surface of the LCD has a coating with 2H hardness to reduce scratching.

10.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 16. Reliability Test>

No.	Items	Condition	Remark
1	HTS/Stg	70° C +/- 3° C, dry,240hr	
2	LTS/Stg	-30° C +/- 3° C, dry,240hr	
3	THS/Stg	60℃, 90%, 240hr, Storage	
4	ACT1/Stg	-40 C to 65° C, 30min dwell,250c	
5	ACT2/Stg	-20 C to 60° C, 15min dwell,250c	
6	HTO)/Op	60° C +/- 3° C, dry,240hr	
7	TC/Op	-10° C to 55° C, dry,250c	
8	LTO/Op	-10° C +/- 3° C, dry,240hr	
9	THO/Op	55℃/85%, 450hr	
10	on/off	30 sec on, 30 sec off, 30000Cycles	
11	push	Tip 5mm, Hold 2s/open 1s, 4~12kgf, 10cycles	
12	VIB	5-500Hz, 2.41Grms, random, +X +Y +Z Sweep 30min	Note 1
13	Shock	240G, 2ms,half sine	
14	altitude	0 - 12,192 m, 24hr	
15	UV exposure	55℃(BP) with light on,8hrs on+4hrs off,10cycles,Daylight-Q , 1120w/m2	
16	Image sticking	5*5 Mosaic Pattern at room temperature	
17	ESD	contact ±15KV,air ±15Kv, pin ±5Kv	Note 1

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.
2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 LABEL

(1) Product Label

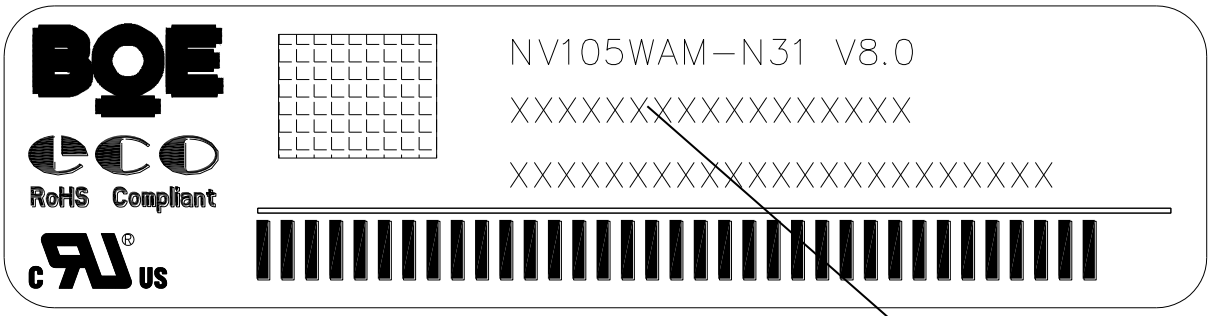


Figure 19. Product Label

Module ID Naming Rule:

<Table 17. Module ID Naming Rule>

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Code	B	9	A	F	1	7	8	8	D	3	1	0	0	0	0	6	8
Description	Product Name		Product Grade	B8	Year		Month	Model Extension Code (Last 4 Digits of FG CODE)				Serial No. 00001-ZZZZZZ					

(2) High voltage caution label

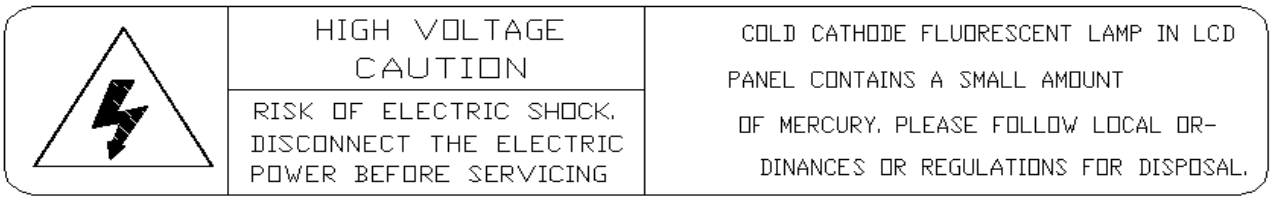


Figure 20. High Voltage Caution Label

(3) Box label

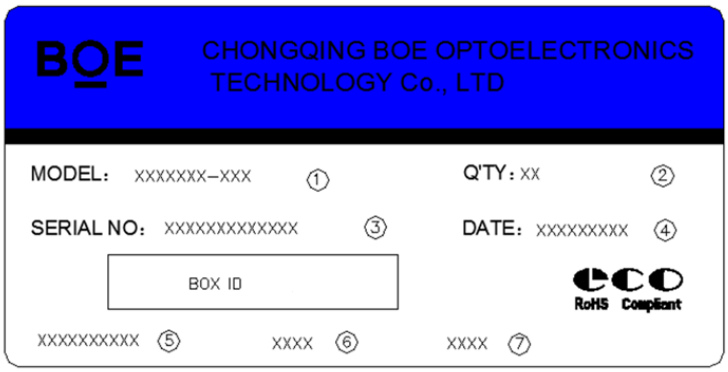


Figure 21. Box Label

Serial number marked part needs to print, show as follows:

1. FG-CODE(Before 12 bit)
2. Product quantity
3. Box ID
4. Date
5. The client section material number(The client)
6. FG-Code After four
7. The supplier code

Total Size:100×50mm

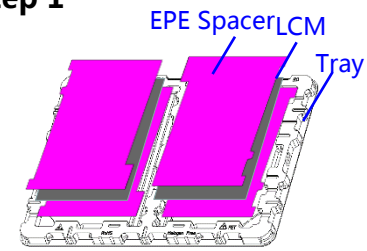
<Table 18. Box Label Naming Rule >

Digit / Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Code	B	9	A	F	1	7	8	N	0	0	3	2	7
Description	Product Name		Product Grade	B8	Year		Month	Revision	BOX Serial Number				

14.0 PACKING INFORMATION

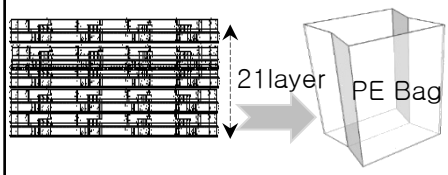
14.1 Packing Order

Step 1



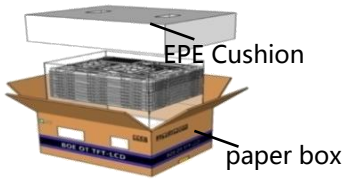
- Put 1 pcs spacer in tray and 1 pcs LCM on spacer, then 1pcs spacer on LCM.
- 2 pcs LCM /tray, 4 pcs spacer/tray.

Step 2



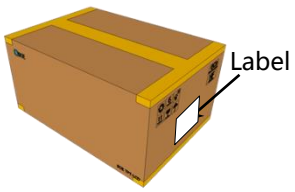
- Put 20+1 pcs trays in PE bag.
- 40 pcs LCM /bag, 80 pcs spacer/bag.

Step 3



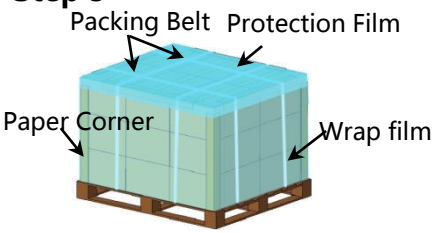
- Put 21 tray + PE bag with 2 EPE cushions in the paper box.
- 40 pcs LCM/paper box.

Step 4



- Sealing Box with packing tape and labeling.

Step 5



- 6ea Box/ layer , 3 layers/pallet .
- Put paper corner and protection film, then wrapping pallet with warp film.
- 720 LCM/18 box/pallet

Step 6

- Double raw and double stack.
- 34560 LCM/48 pallet/track

Figure 22. Packing Order

14.2 Note

- Box dimension: 467mm×351mm×270mm
- Package quantity in one box: 40 pcs
- Total weight: 12.6 kg/Box (typ.)

15.0 MECHANICAL OUTLINE DIMENSION

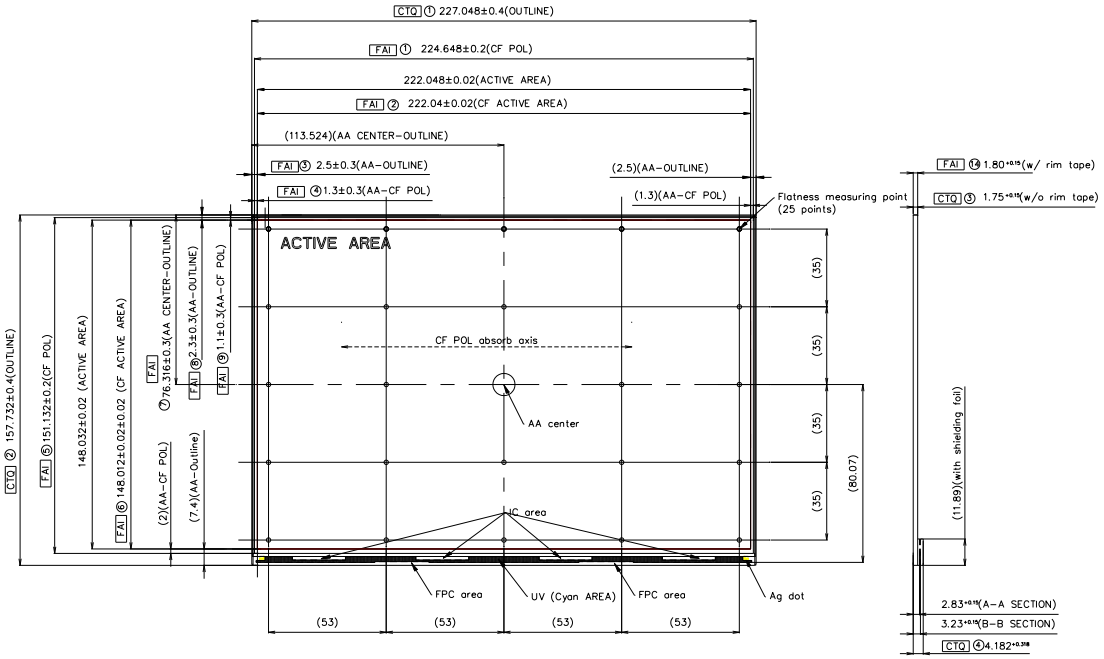


Figure 23. TFT-LCD Module Outline Dimension (Front View)

NOTES:
1.THE eDP CONNECTOR SHOULD BE MEASURED AT CONNECTOR CENTER.
2.FOR UNSPECIFIED DIMENSION, THE TOLERANCE REFER TO ` 0.3 mm
3.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE R EFRE TO PRODUCT SPEC..
4.TOP POLARIZER SHOULD BE THE HIGHEST LEVEL.
5."()" MEANS REFERANCE DIMENSIONS.
6." FAI " MEANS FAI DIMENSION AND IT SHOULD MEASURE 5PCS
7." CTQ " MEANS CTQ DIMENSION AND IT SHOULD MEASURE 32PCS.
8.ALL MATERIALS SHOULD MEET HALOGEN FREE, THE REACH AND ROHS RE QUIREMENT.
9.THE FPC, LGP AND BACK COVER MAY CONTAIN SULFUR AND THE SPECIFIC VALUE WILL BE PROVIDED WHEN THE VENDORS ARE SELECTED.
10.THE LCM FLATNESS(TOP SURFACE) IS 0.6mm MAX.. AND IT SHOULD BE ME ASURED BY COORDINATE MEASURING MACHINE.
11.LCM WEIGHT SPEC: FAI ⑫115g MAX..
12.WARPAGE AND DEFORMATION SPEC.: FAI ⑬ 0.8mm MAX..

Top POL is the highest portion.

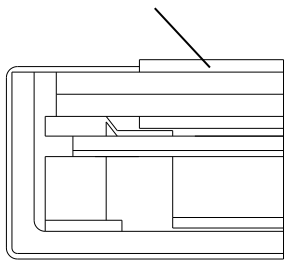


Figure 24. Highest Point Position

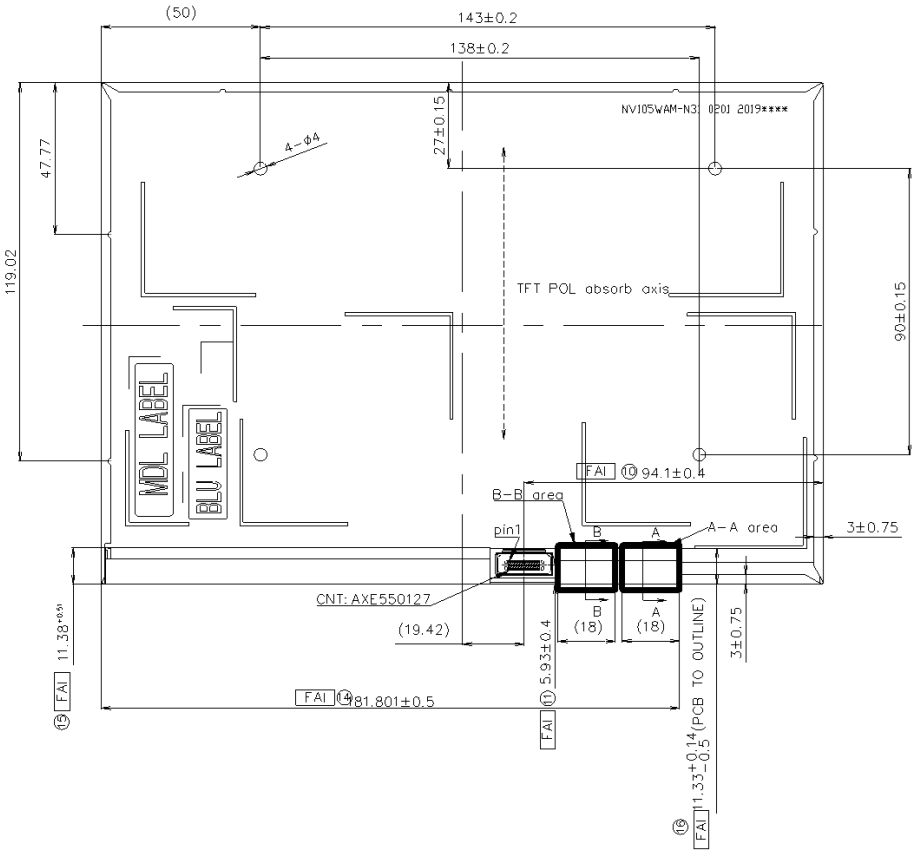


Figure 25. TFT-LCD Module Outline Dimensions (Rear view)

NOTES:

1.THE eDP CONNECTOR SHOULD BE MEASURED AT CONNECTOR CENTER.
2.FOR UNSPECIFIED DIMENSION, THE TOLERANCE REFER TO ` 0.3 mm
3.THE MEASUREMENT METHOD FOR THE DIMENSION OF MODULE, PLEASE REFRE TO PRODUCT SPEC..
4.TOP POLARIZER SHOULD BE THE HIGHEST LEVEL.
5."()" MEANS REFERANCE DIMENSIONS.
6." FAI " MEANS FAI DIMENSION AND IT SHOULD MEASURE 5PCS
7." CTQ " MEANS CTQ DIMENSION AND IT SHOULD MEASURE 32PCS.
8.ALL MATERIALS SHOULD MEET HALOGEN FREE, THE REACH AND ROHS REQUIREMENT.
9.THE FPC, LGP AND BACK COVER MAY CONTAIN SULFUR AND THE SPECIFIC VALUE WILL BE PROVIDED WHEN THE VENDORS ARE SELECTED.
10.THE LCM FLATNESS(TOP SURFACE) IS 0.6mm MAX.. AND IT SHOULD BE MEASURED BY COORDINATE M EASURING MACHINE.
11.LCM WEIGHT SPEC: FAI ⑫115g MAX..
12.WARPAGE AND DEFORMATION SPEC.: FAI ⑬ 0.8mm MAX..

16.0 EDID Table

check		Address (HEX)	Function	Hex	Dec	Input values	Notes
FAE	QE						
-	-	00	Header	00	0	0	EDID Header
-	-	01		FF	255	255	
-	-	02		FF	255	255	
-	-	03		FF	255	255	
-	-	04		FF	255	255	
-	-	05		FF	255	255	
-	-	06		FF	255	255	
-	-	07		00	0	0	
V		08	ID Manufacturer Name	09	9	BOE	ID = BOE
V		09		E5	229		
	V	0A	ID Product Code	8B	139	2187	ID = 2187
	V	0B		08	8		
V		0C	32-bit serial No.	00	0	0	
V		0D		00	0	0	
V		0E		00	0	0	
V		0F		00	0	0	
V		10	Week of manufacture	10	16	16	
V		11	Year of Manufacture	1D	29	2019	Manufactured in 2019
V		12	EDID Structure Ver.	01	1	1	EDID Ver 1.0
V		13	EDID revision #	04	4	4	EDID Rev. 0.4
V	V	14	Video input definition	A5	165	-	Video Signal Interface
	V	15	Max H image size	16	22	22	22cm (Approx)
	V	16	Max V image size	0F	15	15	15cm (Approx)
	V	17	Display Gamma	78	120	2.2	Gamma curve = 2.2
V		18	Feature support	03	3	-	Feature Support
	V	19	Red/Green low bits	9F	159	-	Red / Green Low Bits
	V	1A	Blue/White low bits	15	21	-	Blue / White Low Bits
	V	1B	Red x high bits	A5	165	0.646	Red (x) = 10100101 (0.646)
	V	1C	Red y high bits	54	84	0.329	Red (y) = 01010100 (0.329)
	V	1D	Green x high bits	4C	76	0.300	Green (x) = 01001100 (0.300)
	V	1E	Green y high bits	9C	156	0.612	Green (y) = 10011100 (0.612)
	V	1F	Blue x high bits	27	39	0.152	Blue (x) = 00100111 (0.152)
	V	20	BLue y high bits	10	16	0.063	Blue (y) = 00010000 (0.063)
	V	21	White x high bits	50	80	0.313	White (x) = 01010000 (0.313)
	V	22	White y high bits	54	84	0.329	White (y) = 01010100 (0.329)
V		23	Established timing 1	00	0	-	--
V		24	Established timing 2	00	0	-	
V		25	Established timing 3	00	0	-	

V		26	Standard timing #1	01	1		Not Used
V		27		01	1		
V		28	Standard timing #2	01	1		Not Used
V		29		01	1		
V		2A	Standard timing #3	01	1		Not Used
V		2B		01	1		
V		2C	Standard timing #4	01	1		Not Used
V		2D		01	1		
V		2E	Standard timing #5	01	1		Not Used
V		2F		01	1		
V		30	Standard timing #6	01	1		Not Used
V		31		01	1		
V		32	Standard timing #7	01	1		Not Used
V		33		01	1		
V		34	Standard timing #8	01	1		Not Used
V		35		01	1		
	V	36	Detailed timing/monitor descriptor #1	62	98	164.8	164.82MHz Main clock
	V	37		40	64		
	V	38		80	128	1920	Hor Active = 1920
	V	39		82	130	130	Hor Blanking = 130
	V	3A		70	112	-	4 bits of Hor. Active + 4 bits of Hor. Blanking
	V	3B		00	0	1280	Ver Active = 1280
	V	3C		3C	60	60	Ver Blanking = 60
	V	3D		50	80	-	4 bits of Ver. Active + 4 bits of Ver. Blanking
	V	3E		30	48	48	Hor Sync Offset = 48
	V	3F		20	32	32	H Sync Pulse Width = 32
	V	40		36	54	3	V sync Offset = 3 line
	V	41		00	0	6	V Sync Pulse width : 6 line
	V	42		DE	222	222	Horizontal Image Size = 222.048 mm (Low 8 bits)
	V	43		94	148	148	Vertical Image Size = 148.032 mm (Low 8 bits)
	V	44		00	0	-	4 bits of Hor Image Size + 4 bits of Ver Image Size
	V	45		00	0	0	Hor Border (pixels)
	V	46		00	0	0	Vertical Border (Lines)
	V	47		1A	26	-	Detailed timing Definition

V		48	Detailed timing/monitor descriptor #2	00	0			MHz Main clock
V		49		00	0			
V		4A		00	0			Hor Active =
V		4B		00	0			Hor Blanking =
V		4C		00	0			4 bits of Hor. Active + 4 bits of Hor. Blanking
V		4D		00	0			Ver Active =
V		4E		00	0			Ver Blanking =
V		4F		00	0			4 bits of Ver. Active + 4 bits of Ver. Blanking
V		50		00	0			Hor Sync Offset =
V		51		00	0			H Sync Pulse Width =
V		52		00	0			V sync Offset = line
V		53		00	0			V Sync Pulse width : line
V		54		00	0			Horizontal Image Size = mm (Low 8 bits)
V		55		00	0			Vertical Image Size = mm (Low 8 bits)
V		56		00	0			4 bits of Hor Image Size + 4 bits of Ver Image Size
V		57		00	0			Hor Border (pixels)
V		58		00	0			Vertical Border (Lines)
V		59		1A	26		-	Refer to right above table
V		5A	Detailed timing/monitor descriptor #3	00	0			Indicates descriptor #3 is a display Descriptor
V		5B		00	0			
V		5C		00	0			Reserved
V		5D		FE	254			Tag：ASCII String
V		5E		00	0			Reserved
V		5F		42	66		B	Manufacture name : BOECQ
V		60		4F	79		O	
V		61		45	69		E	
V		62		20	32			
V		63		43	67		C	
V		64		51	81		Q	
V		65		0A	10			
V		66		20	32			
V		67		20	32			
V		68		20	32			
V		69		20	32			
V		6A		20	32			
V		6B		20	32			

V		6C	Detailed timing/monitor descriptor #4	00	0		Indicates descriptor #4 is a display Descriptor
V		6D		00	0		
V		6E		00	0		Reserved
V		6F		FE	254		Tag：ASCII String
V		70		00	0		Reserved
V		71		4E	78	N	Model name : NV105WAM-N31
V		72		56	86	V	
V		73		31	49	1	
V		74		30	48	0	
V		75		35	53	5	
V		76		57	87	W	
V		77		41	65	A	
V		78		4D	77	M	
V		79		2D	45	-	
V		7A		4E	78	N	
V		7B		33	51	3	
V		7C		31	49	1	
V		7D		0A	10		
V	V	7E	Extension flag	00	0	1	Extension flag
-	-	7F	Checksum	C0	192	-	Checksum

Appendix A

The Measurement Methods for the Dimensions of Module

Caliper:

a. Length of Outline

b. Width of Outline (Without/With PCB)

Outline should be measured by caliper on the premise that BOE uses go-no-go tool to control outline by 100%, then the Cpk of outline dimenison is for reference.

Micro-meter:

a. Thickness of Outline (Without/ With PCB)

Coordinate Measuring Machine:

CF Polarizer Size

Active Area Size

Active Area to Outline (Without Tape Wrinkle or Bulged)

Active Area to CF Polarizer

The Distance of Bracket Holes

P-Cover to Outline (Without Tape Wrinkle or Bulged)

Length of P-Cover

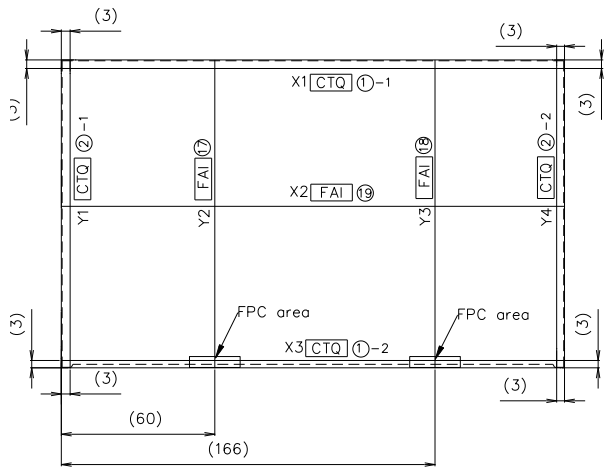
Connector Pin 1 to Outline (Without Tape Wrinkle or Bulged)

Height Gauge: The Different Height of Root and Top on the Bracket
(Need to Calculate From Bracket Angle Spec.)

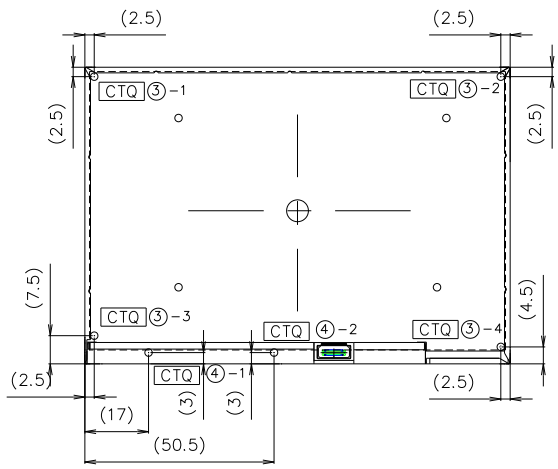
Feeler Gauge: The Warpage Spec. of Module

Notes:

Except the Critical Dimensions as Above, Other Dimensions are Measured by Coordinate Measuring Machine If Necessary.



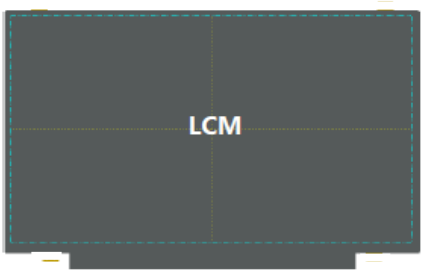
Outline measuring location

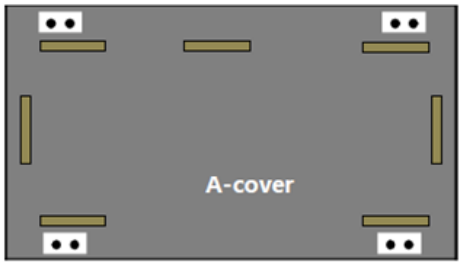


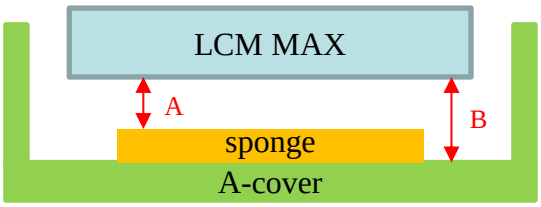
Thickness measuring location

Appendix B

LCM to A-Cover / sponges z-gap







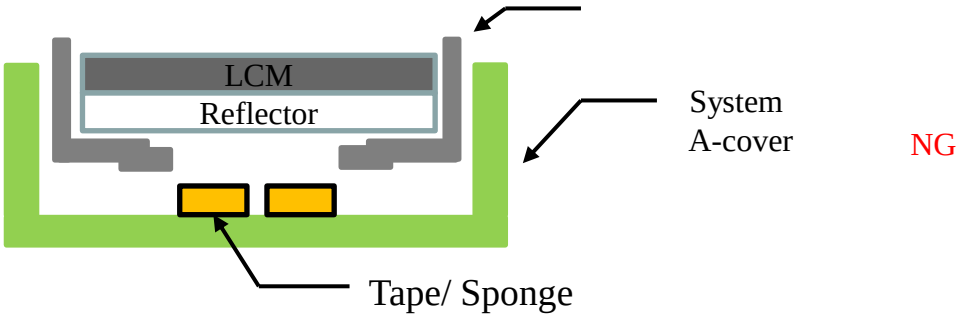
	Plastic Cover (LCM Thickness: Max)	Metal Cover (LCM Thickness: Max)
A	>0mm	>0mm
B	Min: 1.0mm	Min: 0.8mm
Without the open area of back cover		

Purpose	The reflector area is very sensitive, we suggest that design enough z-gap to decrease the risk of water ripple, white spot and other abnormal display

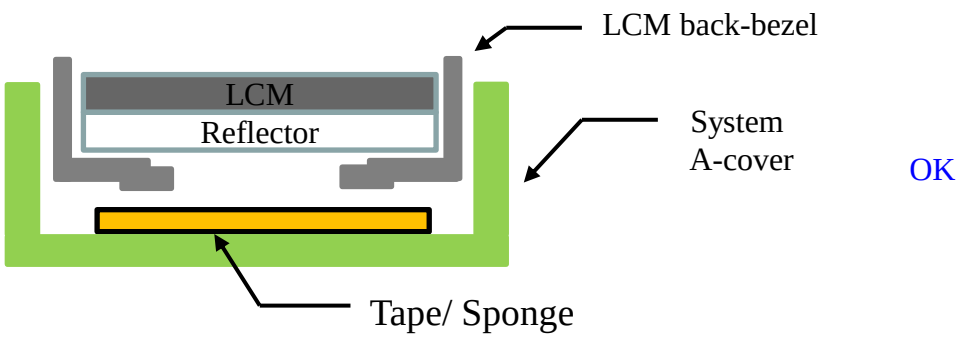
Appendix B

LCM to A-Cover / sponges z-gap

a



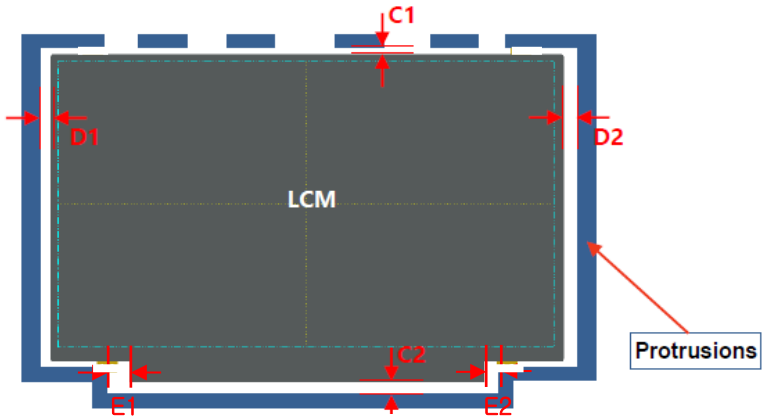
b



Purpose	If attach sponges or rubbers which correspond to white reflector area, it may cause white spot, pooling or other relate issues. We suggest that attach wide range sponges / rubbers which can cover the LCM back-bezel opening

Appendix B

LCM to side wall / protrusions

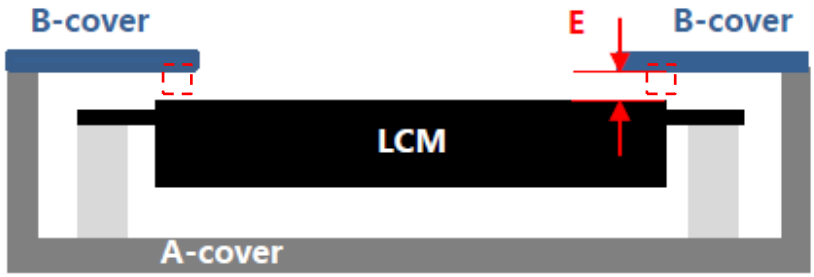


	Normal border	Narrow border
D1/D2	Min: 0.45mm	Min: 0.35mm
C1	Min: 0.50mm	
C2	Min: 0.50mm	
E1/E2	Min: 0.55mm	

Purpose	We suggest that design enough gap around LCM to prevent shock test failure, or interference, cell crack, abnormal display…etc. in the reliability test

Appendix B

LCM to B-cover z-gap

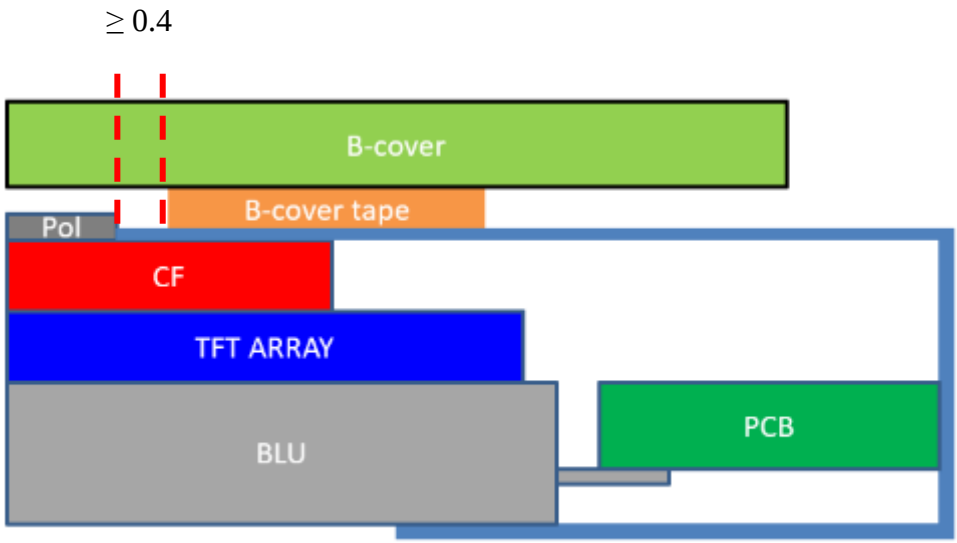


B-cover Tape	Gap
Without	0.15 ~ 0.25mm
With	0.15 ~ 0.20mm

Purpose	Too less z-gap between system B-cover and LCM top pol has high risk to cause cell crack, pooling, light leakage and other issues

Appendix B

B-cover tape to top pol edge

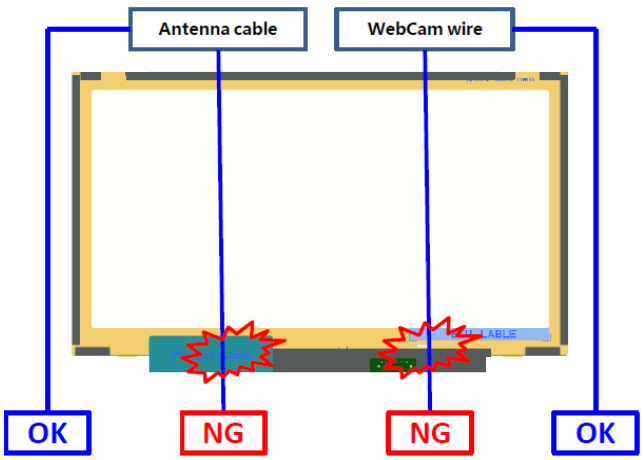


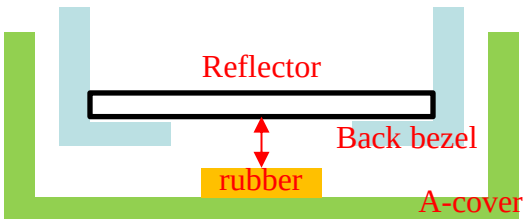
If attach b-cover and LCM with tapes,
Please let tapes to be located out of top pol edges 0.4mm away on 4 sides

Purpose	To avoid the B-cover tape override top pol and cause pooling or light leakage issue

Appendix B

Antenna Cable & Webcam wire



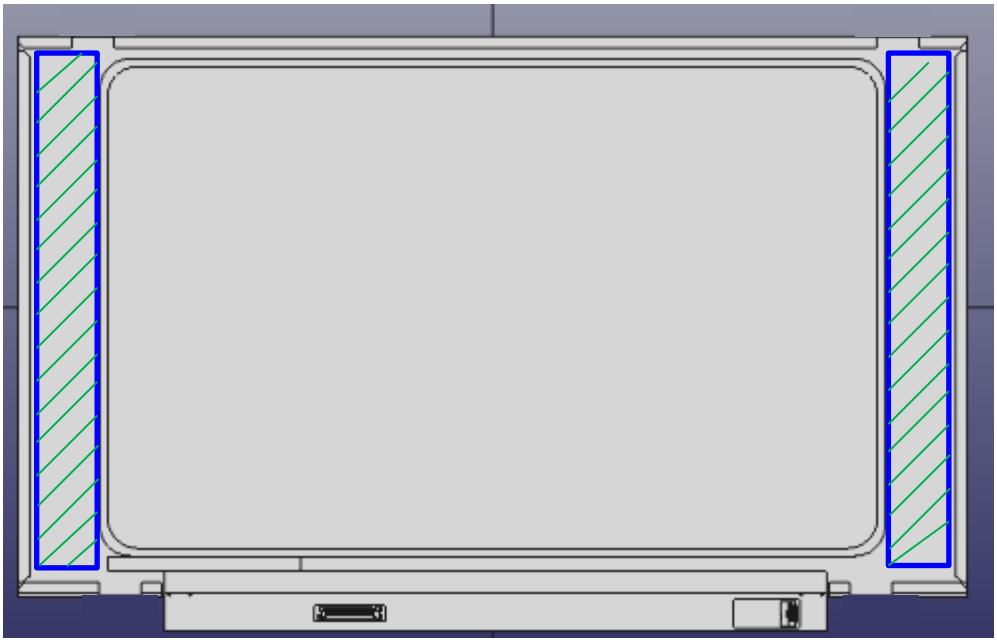


If sponge within the reflector area is necessary, we suggest that the gap between reflector and sponge is more than 0.5mm

Purpose	1. We suggest that do not set Antenna or WebCam cable / wire go behind LCM to avoid backpack test, hinge test ,twist test or pogo test with abnormal display 2. If the cable / wire is necessary to go behind LCM, please make a groove with rounds or chamfers to protect the cable / wire, or attach with higher sponge / rubbers adjacent to the cable / wire route 3. Suggest that attach the cable / wire with tapes to A-cover 4. Do not attach anything with LCM reflector area. If attach cable / wire with LCM reflector area, it may cause pooling, white spot, light leakage and other related issues

Appendix B

LCM paste area

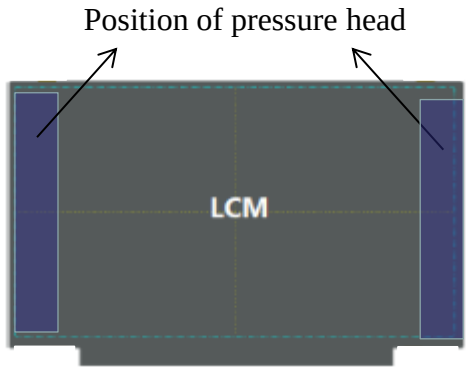


Attachment area

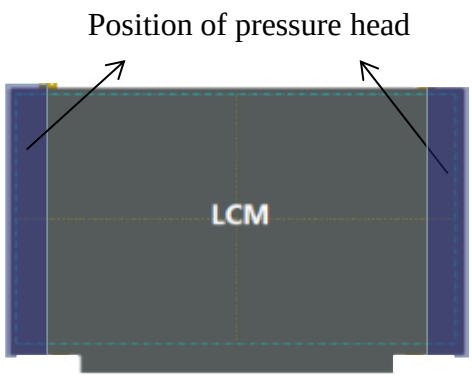
Purpose	If use the stretch remove tapes to fix LCM with A-cover, please set the stretch remove tapes correspond to the LCM back-bezel and do not let the tapes override the back-bezel's level step of opening

Appendix B

LCM pressable area



NG

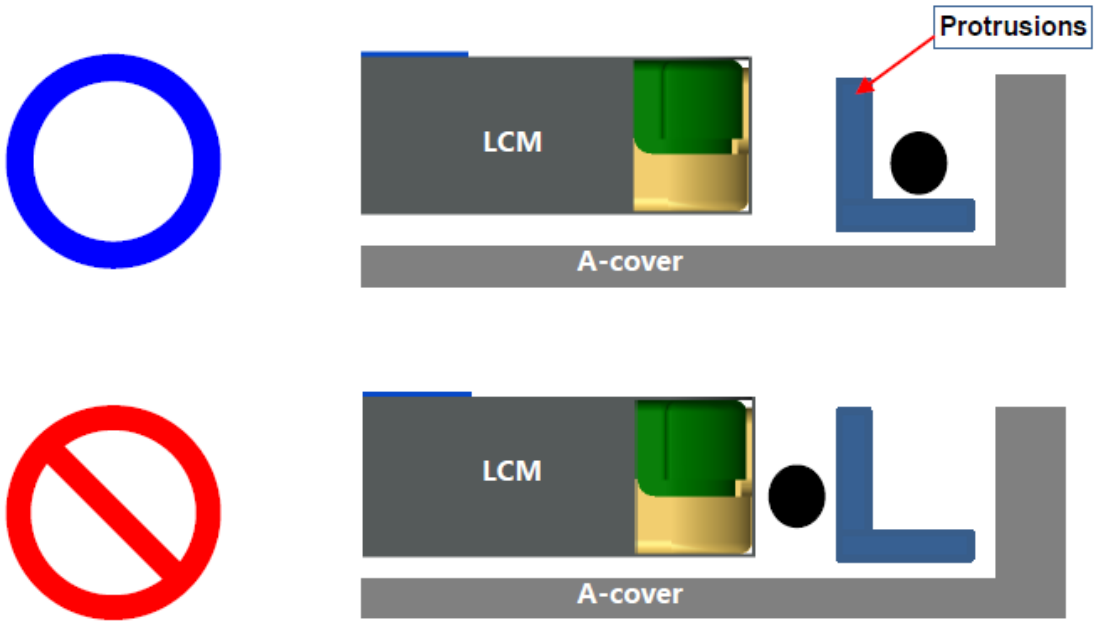


OK

Purpose	1. LCM is fixed on A-cover by double-sided tap which can stick LCM after using the press jig stress LCM during assembling. 2. To avoid panel broken the design of pressure head of press jig can not only pin on cell panel. The pressure head needs to pin on the LCM frame, which the LCM frame can share the pressure of the pressing head.

Appendix B

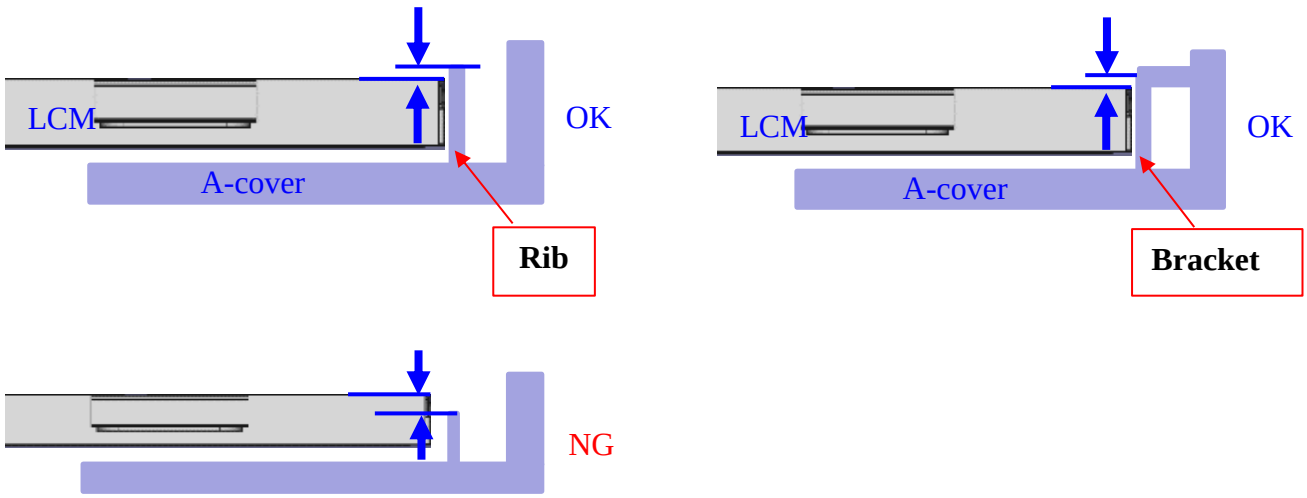
Wire setting



Purpose	Wire should be placed between Protrusions and A-cover. If place the wire between LCM and Protrusions, it may interfere with LCM when assembling B-covers, or even cause LCM breakage in reliability test.

Appendix B

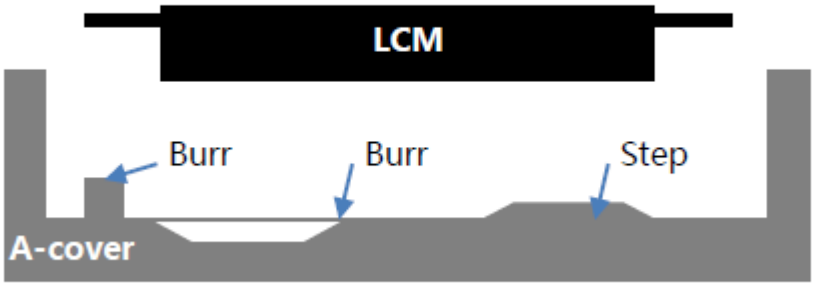
A-cover strength



Purpose	1. It is recommended that Rib height is higher than LCM, in order to avoiding press on LCM edge panels. 2. As for LCM is more stronger than Rib, the L Bracket is be recommended.

Appendix B

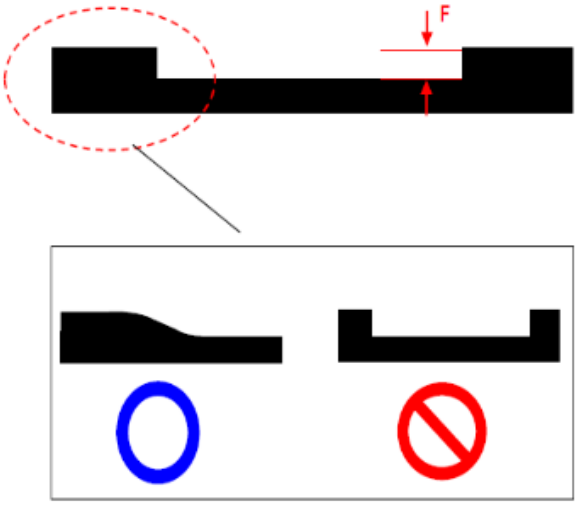
System A-cover Inner Surface



Purpose	There should not exist any burr, segment gap or protrusions beside Logo, which would cause White Spot or Glass Broken by stress concentration.

Appendix B

Keyboard area & Mouse pad

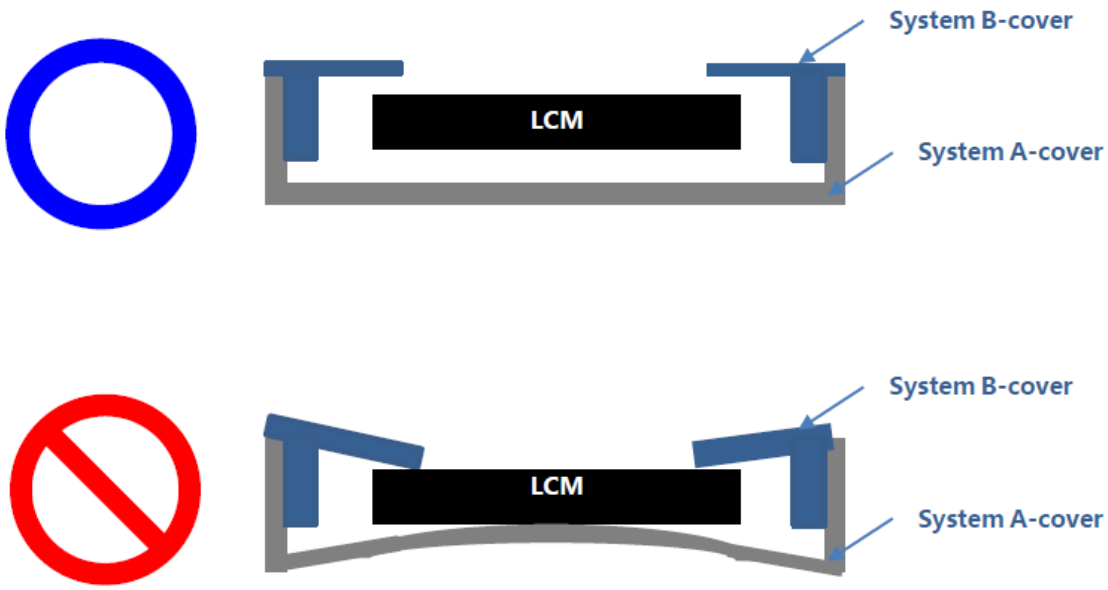


- F: max 0.3mm

Purpose	In order to avoiding LCM fragments in reliability test, the step surface of Keyboard and Mouse pad transmits smoothly, and should not be right-angle. For example, when Pogo testing, if the broken hole is done in this location, it is easy to produce fragments.

Appendix B

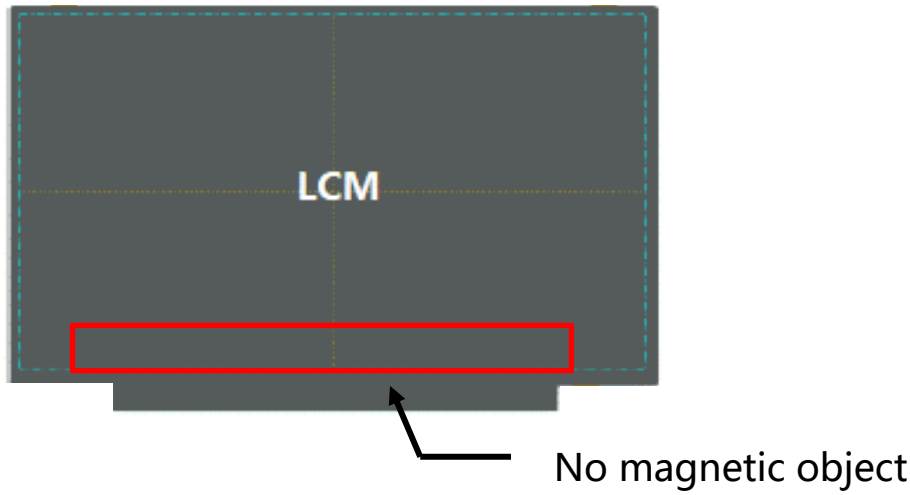
System cover reliability



Purpose	The permanent deformation part of System cover after the reliability test, including sponge and other structures or components, can not touch LCM.

Appendix B

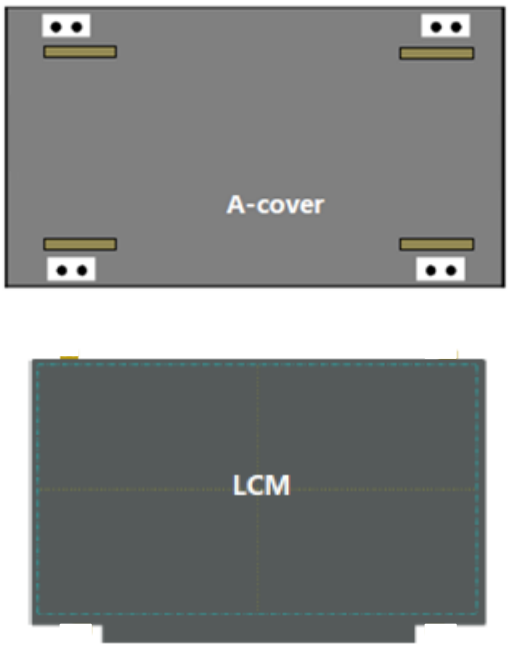
A/B-cover near LCD PCBA



Purpose	There should not have magnet object near LCM PCBA, which is prone to cause physical or electricity noise issue

Appendix B

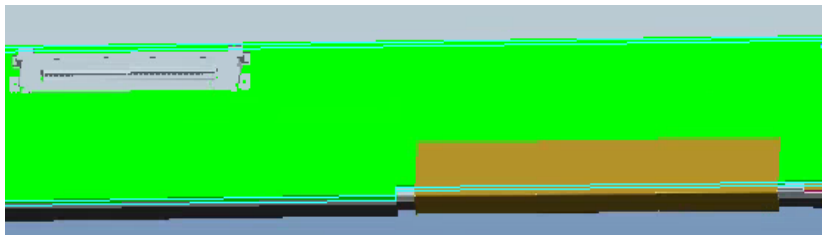
A-cover add sponges on Boss side wall

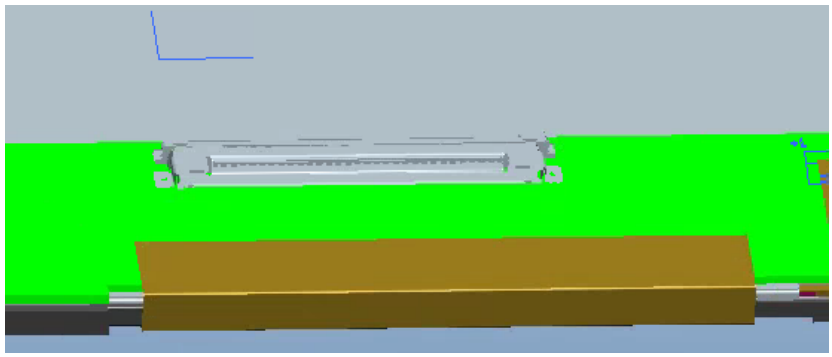


Purpose	We suggest to attach Sponges to the side of the Boss column of A-cover to reduce the panel broken possibility in assembly. It is recommended to this design synchronously.

Appendix B

LCM to A-Cover / sponges z-gap

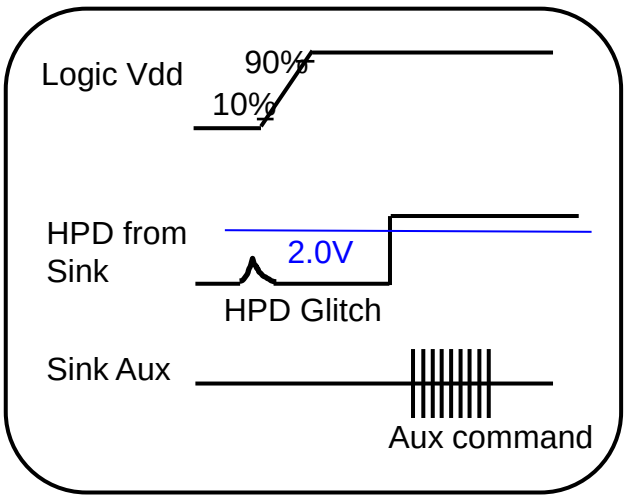




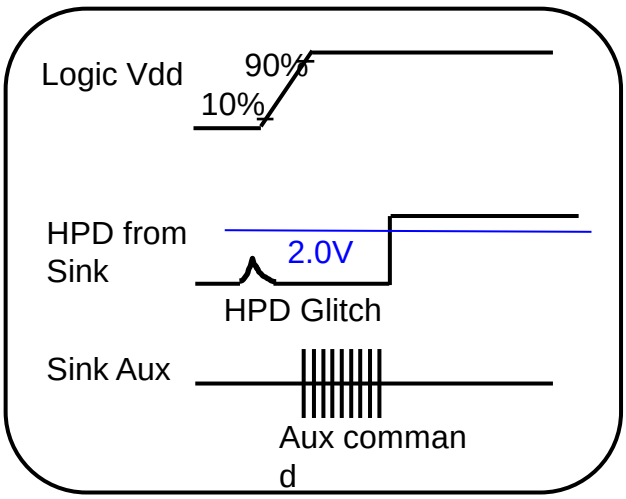
Purpose	Bent product: The position of system connector and FPC should be staggered in X direction. Otherwise, when testing, the system Cable line extrudes FPC, leading to FPC Crack; (Panel FPC Bonding location is related to Mask and can not be changed easily)

Appendix C

HPD Signal recognition



Normal Signal (Ignore HPD Glitch)

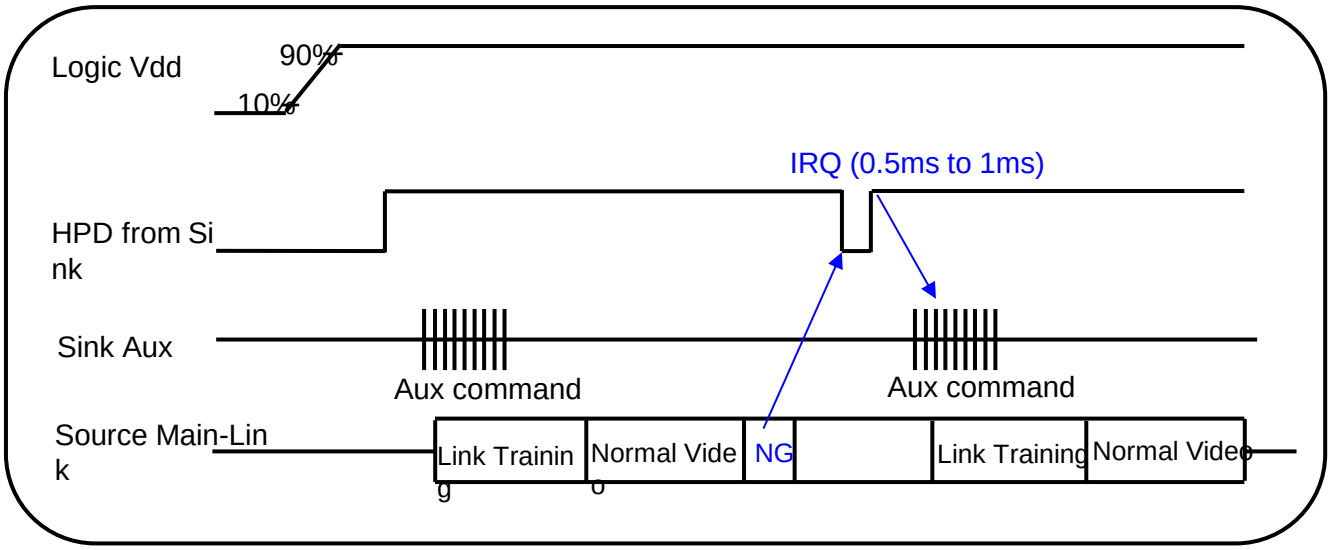


Abnormal Signal

Purpose	When HPD glitch of source device minimum is 2.0(V).

Appendix C

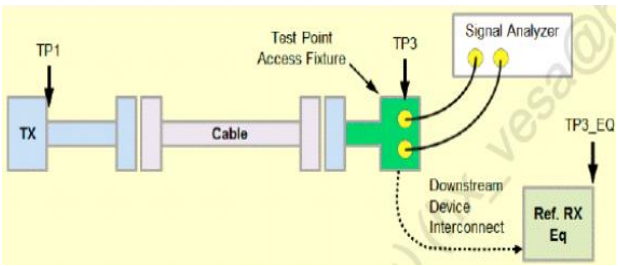
HPD Signal Definition IRQ (Interrupt Request)



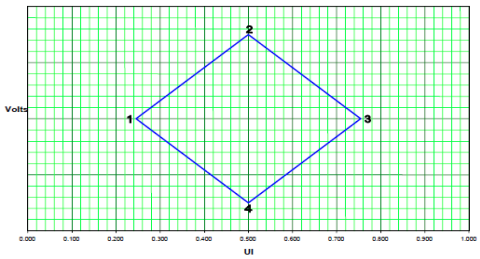
Purpose	When HPD signal low than 0.5ms to 1ms, the source device should check sink status field from the DPCD and take link training again.

Appendix C

Main link eye diagram of TP3



Measured TP3 on LCM connector.



Downstream Device Mask at TP3

	UI	Voltage
1	0.246	0
2	0.5	0.075
3	0.755	0
4	0.5	-0.075

Eye for TP3 at HBR

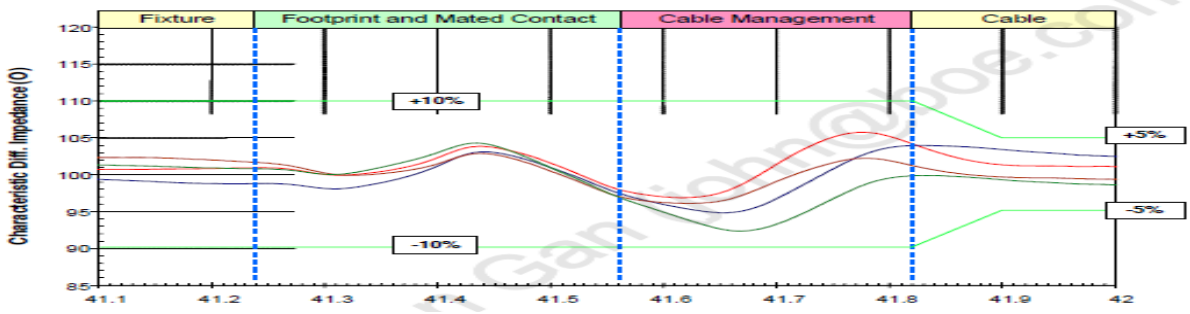
	UI	Voltage
1	0.375	0
2	0.5	0.023
3	0.625	0
4	0.5	-0.023

Eye for TP3 at RBR

Purpose	1. Main Link EYE Diagram should meet TP3 point of VESA. 2. The measure method is through access fixture.

Appendix C

Impedance Profile through a DP Connector



Differential Impedance Profile Measurement Data Example

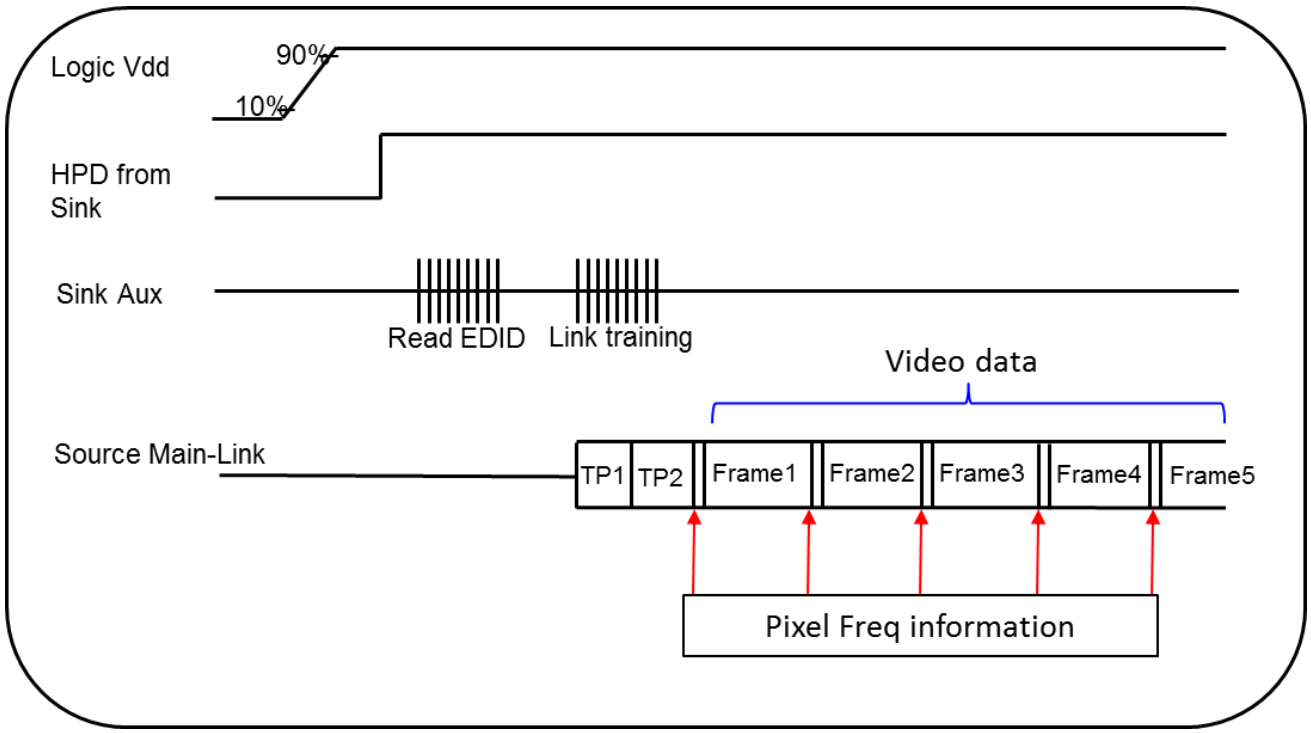
Segment	Differential Impedance Value	Maximum Tolerance
Fixture	100Ω/85Ω VESA	±10%
Connector	100Ω/85Ω VESA	±10%
Wire management	100Ω/85Ω VESA	±10%
Cable	100Ω/85Ω VESA	±5%

Impedance Profile Values for Cable Assembly

Purpose	Cable Impedance Profile 100ohm for Cable Assembly

Appendix C

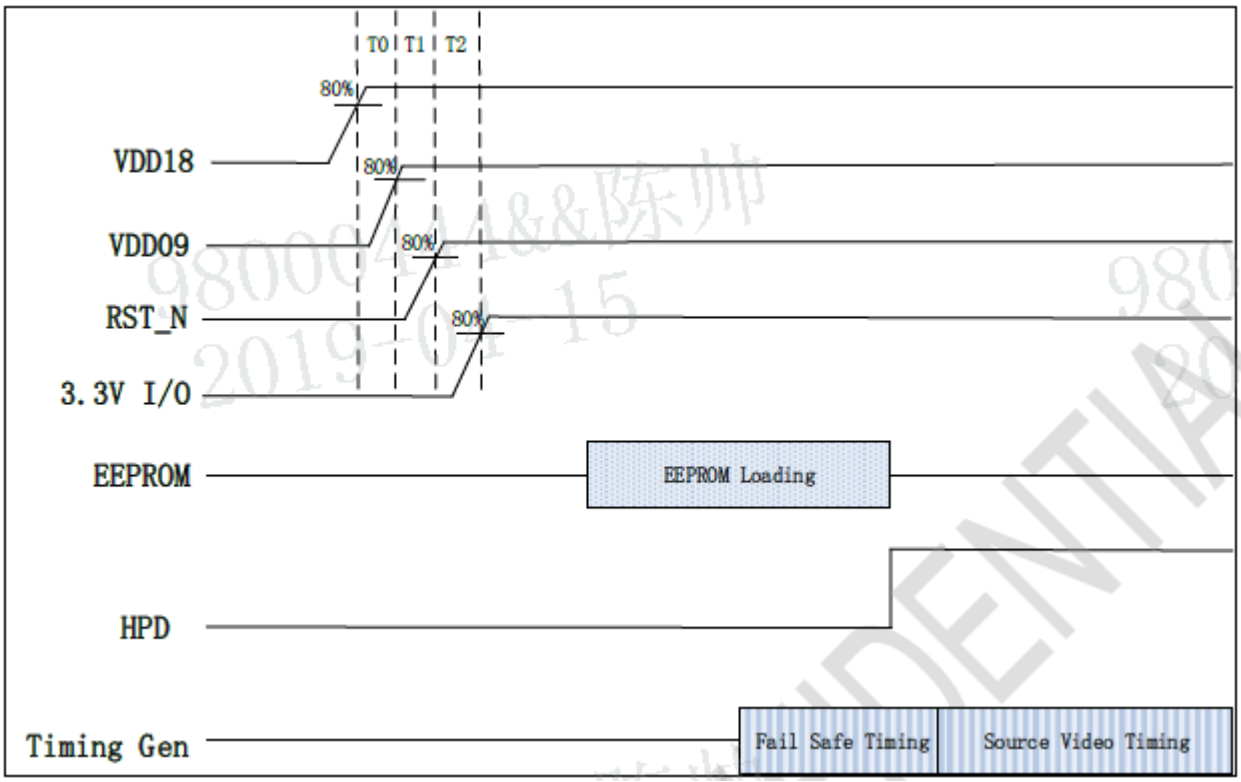
Main Link Pixel Freq information value of MSA data



Purpose	1. It need to fix pixel freq information value of MSA data output to prevent the initial abnormal pixel freq information value from incoming after power on. 2. BOE can read DPCD to check this value. Ex: BIOS is 1.62G , but into windows is 2.7G.

Appendix D

TCON POWER ON SEQUENCE



Symbol	Parameter	Min	Typ	Max	Unit
T0	Interval between VDD18 and VDD09	0.5	—	—	ms
T1	Interval between VDD09 and RST_N	0.5	—	—	ms
T2	Interval between RST_N and 3.3V I/O (PWM_IN, DBC_EN, BIST_EN and LOGO_EN)	1	—	—	ms
V_{th}	RST_N high level threshold	1.44	—	—	V

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.