深圳市智诚光电发展有限公司

APPROVAL SHEET

承 认 书

客户名称 Customer	
产品型号 Part NO.	**ZC156IA02**
产品内容 Product type	Mode: TFT LCD Module
备注栏 Remarks	□APPROVAL FOR SEPCIFICATIONS ONLY ■APPROVAL FOR SEPCIFICATIONS AND SAMPLE
客户确认签章 Signature by Customer:	
备注/ Notes:	

PREPARED BY	CHECKED BY	APPROVED BY

RECORDS OF REVISION

DATE	NO	REVISED No.	PAGE	SUMMARY	NOTE
2022-10-11		Rev01		-	

1. Application

This specification applies to a color TFT-LCD Module,

2. Overview

This Open-cell is a color active matrix LCD open-cell incorporating Oxide TFT (Thin Film Transistor).It is composed of a color TFT-LCD panel, driver ICs, a control circuit and power supply circuit. Graphics and texts can be displayed on a 1920×3×1080 dots panel with 16.7M(8bit) colors by using eDP (Embedded Display Port) Ver1.2 interface and supplying +3.3V DC supply voltage for TFT-LCD panel driving.

In this TFT-LCD panel, color filters for excellent color performance is incorporated to realize brighter and clearer pictures, making this open-cell optimum for use in multi-media applications.

Optimum viewings are in all directions.

Without Backlight-driving LED controller.

eDP transfer rate specification: 2.7Gbps/2 lane 8bit

3. Mechanical specifications.

Parameter	Specification	Unit	Note
Display size	15.6” (Diagonal)	inch	
Active area	344.16(H) ×193.59(V)	mm	
Pixel Format	1920(H) ×1080(V) （1pixel = R + G + B dot）	pixel	
Pixel pitch	0.17925(H) x 0.17925 (V)	mm	
Pixel configuration	R, G, B vertical stripe		
Display mode	Normally black		
Power Consumption	2.94	W	
Surface treatment of front polarizer	Anti-glare coating: (3H)		

Outline dimensions

Parameter		Min	Typ	Max	Unit	Remark
Unit outline dimensions	Width	350.46	350.76	351.06	mm	
	Height	204.66	204.96	205.26	mm	
	Depth	2.7	2.9	3.1	mm	w/o PWB.[Note3-2]
Mass		-	-	-	g	

[Note 3-1]Outline dimensions is shown in page 19

[Note 3-2]Without war page and deflection.

4. Input Terminals

4-1 Driving interface of PWB

CN1 (eDP signals，+3.3V DC power supply and B/L power supply)

Pin No.	Symbol	I/O	Function	Remark
1	NC	-	Reserved for CD	[Note4-1-1]
2	H_GND	P	High Speed round	[Note4-1-2]
3	Lane1_N	I	Complement Signal Link Lane 1	
4	Lane1_P	I	True Signal Link Lane 1	
5	H_GND	P	High Speed round	[Note4-1-2]
6	Lane0_N	I	Complement Signal Link Lane 0	
7	Lane0_P	I	True Signal Link Lane 0	
8	H_GND	P	High Speed round	[Note4-1-2]
9	AUX_CH_P	I	True Signal Auxiliary Channel	
10	AUX_CH_N	I	Complement Signal Auxiliary Channel	
11	H_GND	P	High Speed round	[Note4-1-2]
12	LCD_VDD	P	LCD logic and driver power(3.3V)	
13	LCD_VDD	P	LCD logic and driver power(3.3V)	
14	NC	I	Reserved for LCD manufacturer's use	[Note4-1-1]
15	LCD_GND	P	LCD logic and driver ground	
16	LCD_GND	P	LCD logic and driver ground	
17	HPD	O	HPD signal pin	
18	LED-1	P	Backlight ground	
19	LED-2	P	Backlight ground	
20	LED-3	P	Backlight ground	
21	LED-4	P	Backlight ground	
22	BL_ENABLE	I	Backlight on/off	
23	BL_PWM_DIM	I	System PWM	
24	NC	-	Reserved for LCD manufacturer's use	[Note4-1-1]
25	NC	-	Reserved for LCD manufacturer's use	[Note4-1-1]
26	BL_PWR	P	Backlight power	
27	BL_PWR	P	Backlight power	
28	BL_PWR	P	Backlight power	
29	BL_PWR	P	Backlight power	
30	NC	-	Reserved for LCD manufacturer's use	[Note4-1-1]

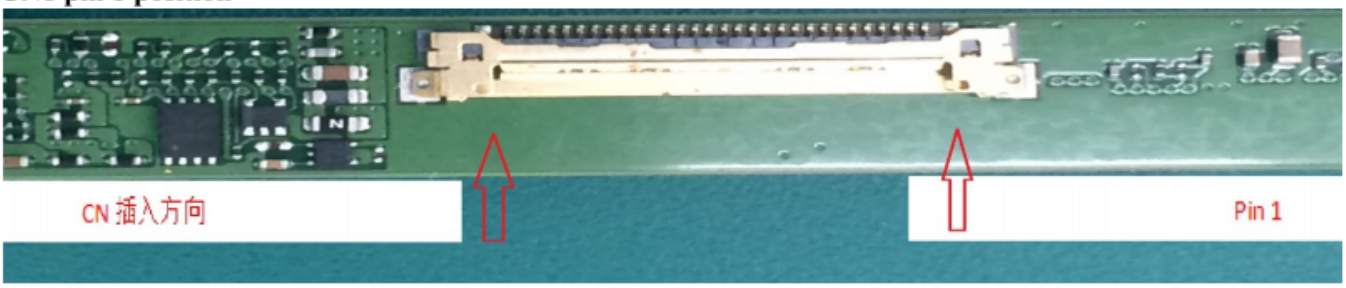
*1 P: POWER I: Input O: Output

[Note 4-1-1] Don't input any signals or any powers into a NC pin. Keep the NC pin open.
[Note 4-1-2] The shielding case is connected with signal GND.

- Connector used :20455-030E-76(I-PEX)
- Corresponding connector : 20453-030T (I-PEX)

(Panda is not responsible to its product quality, if the user applies a connector not corresponding to the above model.)

CN1 pin 1 position



4-2 eDP interface

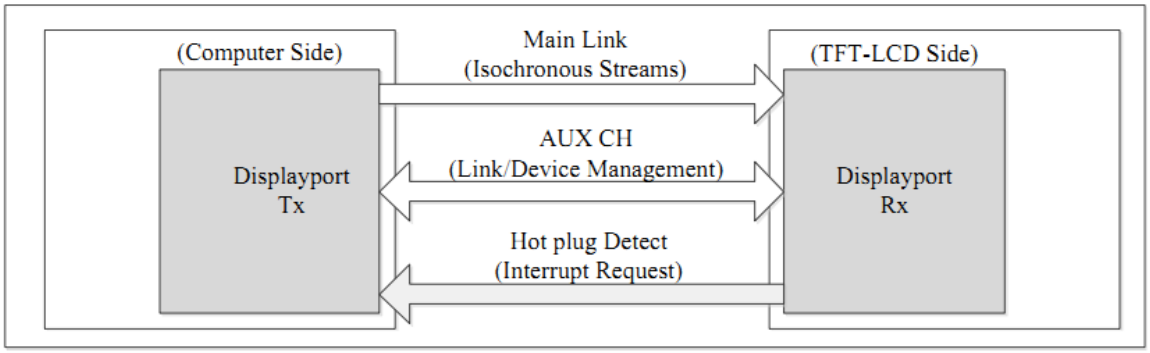


Fig.4-2-1 DP architecture

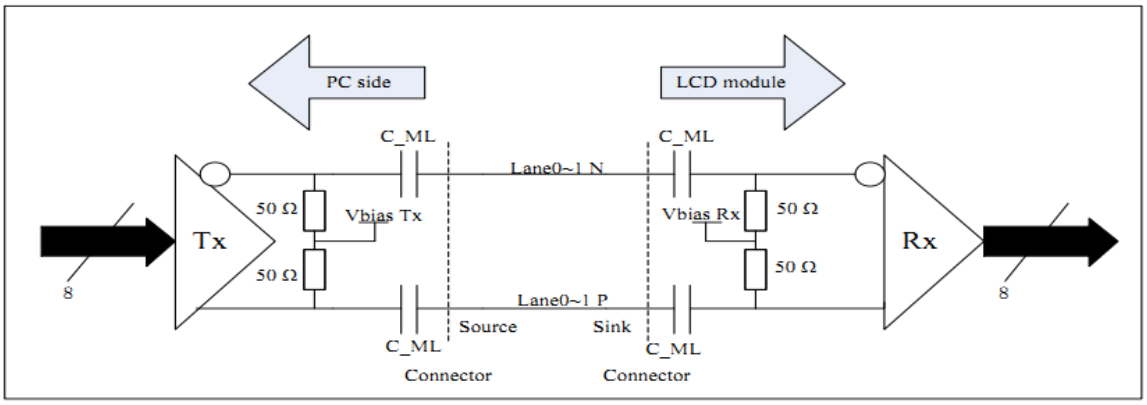


Fig.4-2-2 Main Link differential pair

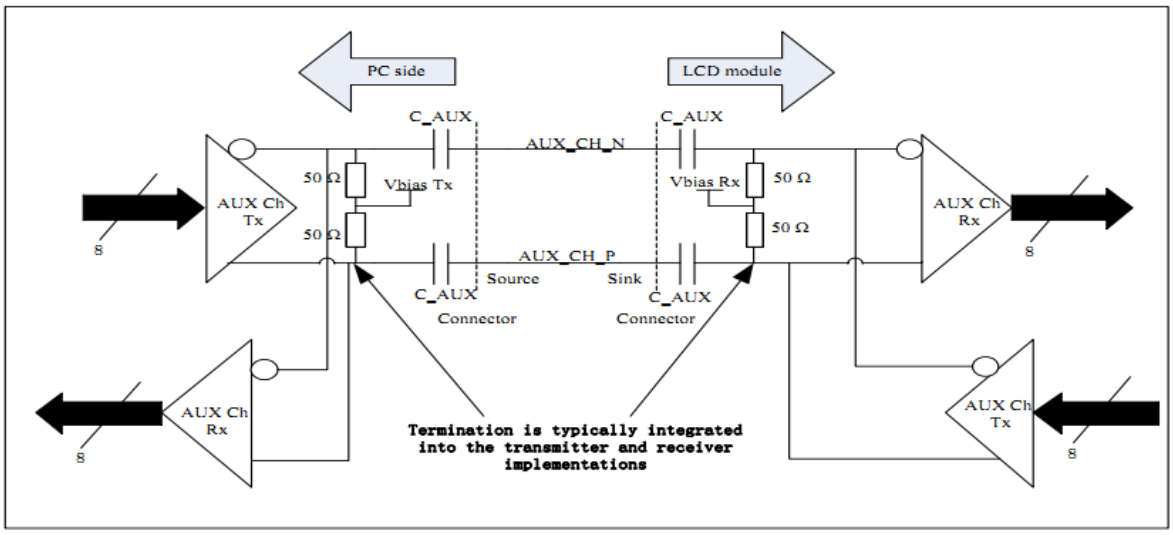


Fig.4-2-3 AUX Link differential pair

Lane0	Lane1	Lane2	Lane3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

Fig.4-2-4 eDP 2lane 8bit input data mapping

5. Electrical Characteristics

5-1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings		Unit	Remark
			MIN	MAX		
+3.3V supply voltage	VDD	Ta=25℃	-0.3	+4.0	V	
Backlight supply voltage	V_{BL}	Ta=25℃	-0.3	+26	V	
Input voltage(eDP)	VI	Ta=25℃	-0.3	+1.5	V	[Note 5-1]
Input voltage(BL)	V_{BL}_I	Ta=25℃	-0.3	VDD+0.3	V	[Note 5-2]
Operation temperature	Topa		0	+50	℃	[Note 5-3]
Storage temperature	Tstg		-20	+60	℃	

(*) “Absolute Maximum Ratings” is regulations that do not exceed it even momentarily.

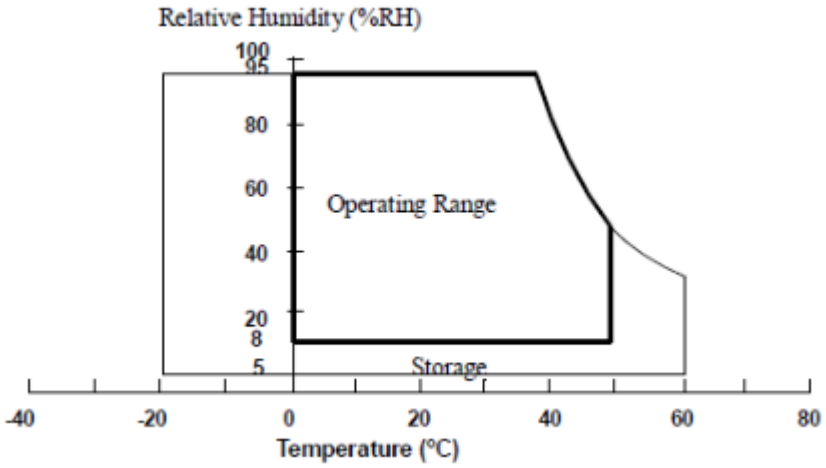
(*) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

[Note 5-1] eDP signals

[Note 5-2]Backlight control signals (BL_ENABLE,BL_PWM_DIM)

[Note 5-3] Humidity: 90%RH Max.at Ta≦+40℃.

Maximum wet-bulb temperature at +39℃ or less at Ta>+40℃, No condensation.

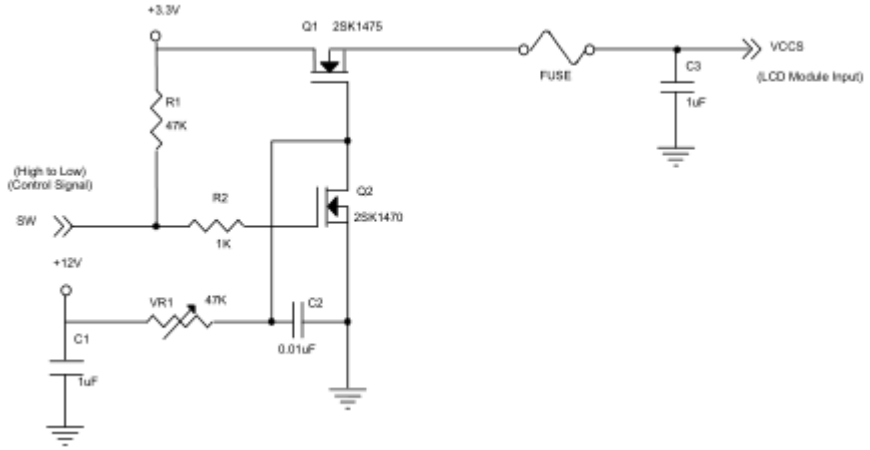


5. DC Characteristics

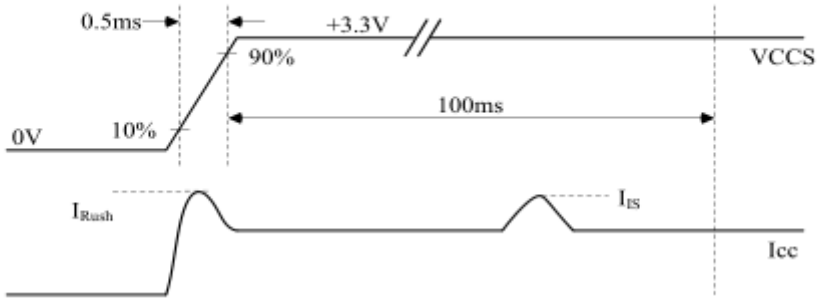
5-2-1. TFT-LCD panel driving

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
Ripple Voltage		V_{RP}	-	50	150	mV	(1)
Inrush Current		I_{RUSH}	0	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	I_{VCCS}	210	240	270	mA	(3)
	Black		190	220	250	mA	(3)
	H 1 line Stripe		450	550	650	mA	
HPD Pull-Low Resistance		R_{HPD}	30K	-	100K	ohm	(4)
HPD	High Level	VH_{HPD}	2.25	-	2.75	V	(5)
	Low Level	VL_{HPD}	0	-	0.4	V	(5)

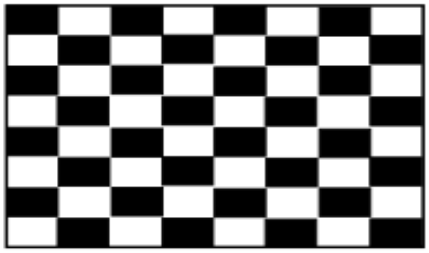
Note (1) The ambient temperature is Ta = 25 ± 2 ºC.
Note (2) I RUSH : the maximum current when VCCS is rising
IIS : the maximum current of the first 100ms after power-on
Measurement Conditions: Shown as the following figure. Test pattern: black.



VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f v = 60 Hz, whereas a specified power dissipation check mosaic pattern is displayed Mosaic Pattern



Active Area

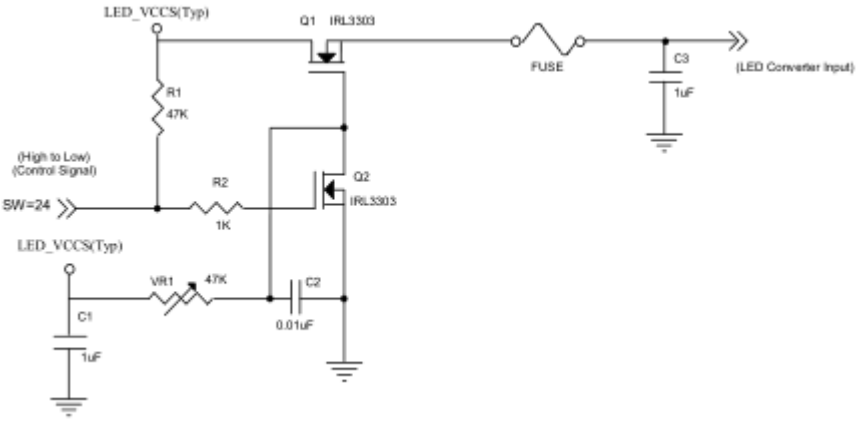
Note (4) The specified signals have pull down resistor to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more information.
Note (5) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action.

6 . Backlight driving

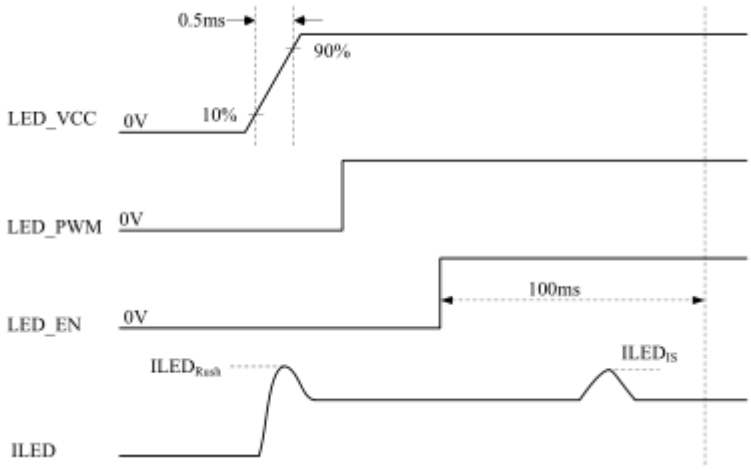
The backlight system is an edge-lighting type with white-LED.
(It is usually required to measure under the following condition: Ta=25℃±2℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	V_{BL}	7.0	12.0	21.0	V	
Current dissipation	I_{BL}	-		1.5	A	V_{BL}=12V Duty Ratio=100%
LED-BL ON/OFF High voltage	$V_{CNT}H$	2.2	-	5.0	V	[Note6-3-3]
LED-BL ON/OFF low voltage	$V_{CNT}L$	0	-	0.6	V	
LED_EN Pull-Low Resistance	R_{LED_EN}	30k	-	100k	ohm	
Modulated light signal voltage	$V_{PWM}H$	2.2	-	5.0	V	
	$V_{PWM}L$	0	-	0.6	V	
PWM Pull-Low Resistance	R_{pwm}	30k	-	100k	ohm	
PWM Control Permissive Ripple	Duty	1	-	100	%	[Note6-3-1]
Brightness Control pulse width Voltage	V_{PWM_pp}	0	-	100mV	μs	Note6-3-2]
Brightness Control frequency	f_{PWM}	190	-	2,000	Hz	
LED lifetime	-	-	20,000	-	h	LED

Note (1) ILED RUSH : the maximum current when LED_VCCS is rising,
ILED IS : the maximum current of the first 100ms after power-on,
Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f PWM= 200 Hz, Duty=100%



VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it’s a suggestion that PWM control frequency should follow the criterion as below.
PWM control frequency f PWM should be in the range

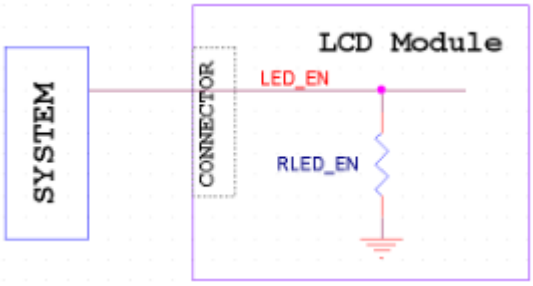
$$(N+0.33)*f \le f_{PWM} \le (N+0.66)*f$$

N : Integer $(N \ge 3)$

f : Frame rate

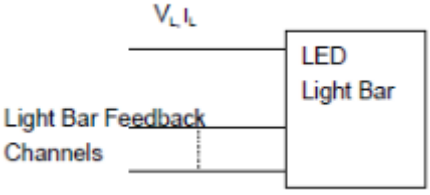
Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, Ta = 25± 2 ºC, fPWM = 200 Hz, Duty=100%.

Note (4) The specified signals have pull down resistor to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down resistance of LED_EN (If it exists). The rest pull down resistance of other signals (eg. HPD, PWM …) are in the same concept.



Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low,slight brightness change might be observed.

Note (6) LED Light Bar Power Supply Current is measured by utilizing a high frequency current meter as shown below



Note (7) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with
current balancing function to drive LED light-bar.

Note (8) VLOVP=35V.

7. Timing characteristics of input signals

7-1.Timing Characteristics

The input signal timing specifications are shown as the following table and timing diagram.

Refresh rate 60Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	151.6	152.84	154.04	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2240	2250	2260	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

Refresh rate 50Hz (Power Saving Mode)

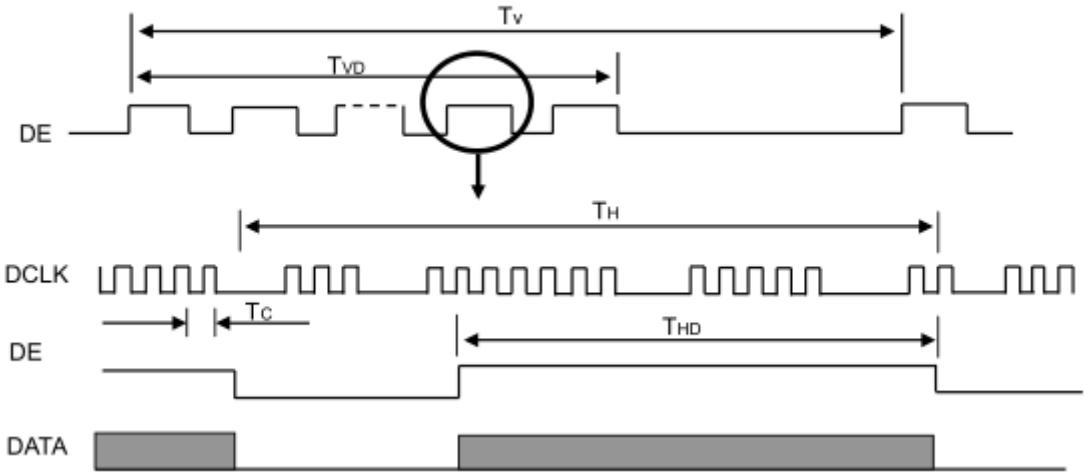
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	126.35	127.35	128.35	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2240	2250	2260	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

Refresh rate 50Hz (Power Saving Mode)

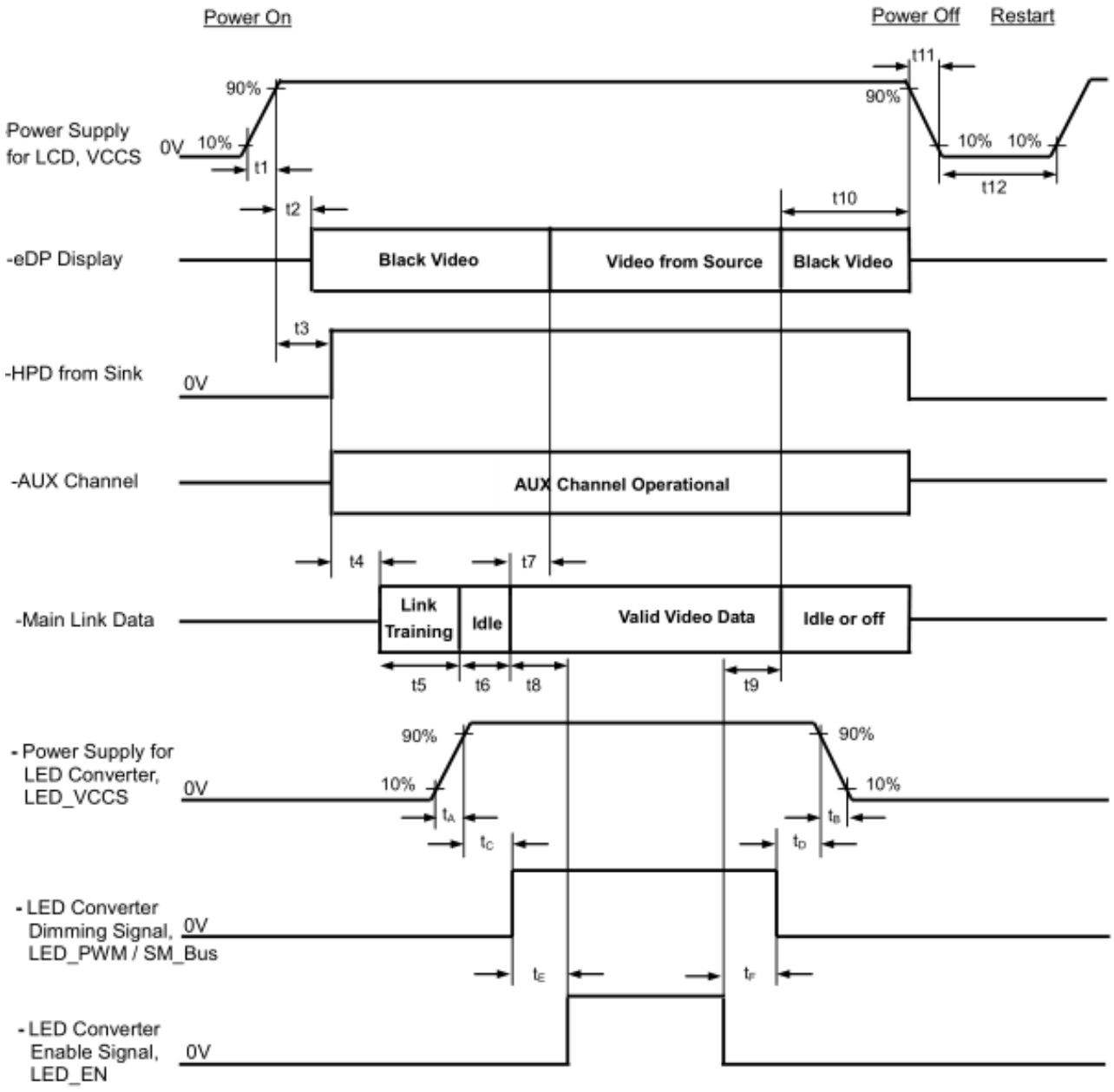
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	121.3	122.26	123.22	MHz	-
DE	Vertical Total Time	TV	1128	1132	1136	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	52	TV-TVD	TH	-
	Horizontal Total Time	TH	2240	2250	2260	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	330	TH-THD	Tc	-

Note (1) The panel can operate at 60Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 60Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

INPUT SIGNAL TIMING DIAGRAM



7-2. POWER ON/OFF SEQUENCE



Timing Specifications:

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	500	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	500	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	500	ms	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	500	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	500	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	See Note 5 below

t12	VCCS Power off time	Source	500	-	ms	-
tA	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
tB	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
tC	Delay from LED power rising to LED dimming signal	Source	1	500	ms	-
tD	Delay from LED dimming signal to LED power falling	Source	1	500	ms	-
tE	Delay from LED dimming signal to LED enable signal	Source	1	500	ms	-
tF	Delay from LED enable signal to LED dimming signal	Source	1	500	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCD VCCS power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCD VCCS power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

. Note (5) The VCCS power rail is recommended to rise and fall linearly. If not, please contact us to conduct risk assessment.

7-3. Input data signals and display position on the screen

Display position of input data(VH)

7-4 Input sigal,basic display colors and gray scale of each color

	Colors & Gray Scale	Gray Scale	Data signal																							
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
			LSB							MSB	LSB							MSB	LSB							MSB
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

0: Low level voltage, 1: High level voltage.

Each basic color can be displayed in 256 gray scales from 8 bit data signals.
According to the combination of 24 bit data signals, the 16.7M color display can be achieved on the screen.

8. EDID Specifications (TBD)

9. Optical characteristics

Paramete	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle (CR>10)	Horizontal	θL	80	85	-	degree	[Note9-1,9-3,9-4,9-6]
		θR	80	85	-		
	Vertical	θT	80	85	-		
		θB	80	85	-		
Contrast Ratio	Center		800	1000	-	-	[Note9-2,9-4,10-6]
Response Time	Tr+Td		-	25	30	ms	[Note9-1,9-5,9-6]
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.05	-	Typ. +0.05	-	[Note 9-2,9-6] Normal operation (PWM Duty=100%)
	Red y			-		-	
	Green x			-		-	
	Green y			-		-	
	Blue x			-		-	
	Blue y			-		-	
	White x			-		-	
	White y			-		-	
Color temperature	Tc		-	-	-	-	
NTSC ratio	%			(45)		-	
Center Luminance of white	Y_{LI}		250	280		cd/m	
White uniformity	δ_W		75	80			[Note 9-2,9-7]

※The measurement shall be taken 30 minutes after lighting the module at the following rating.
※Condition: PWM Duty = 100%
※The optical characteristics shall be measured in a dark room or equivalent.

[Note 9-1] Measurement of viewing angle range [Note 9-2] Measurement of luminance and Response time. Chromaticity and Contrast.

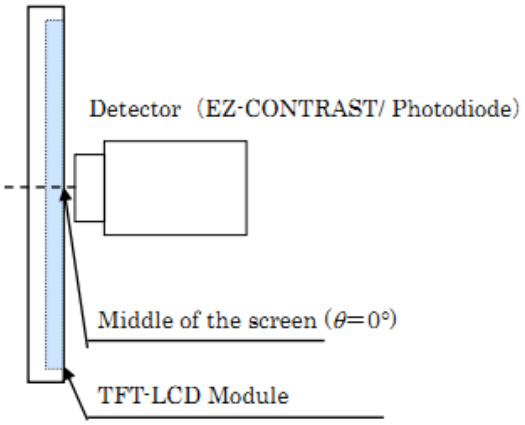


Fig.9-1 Measurement of Viewing angle range and Response time.
(Viewing angle range: EZ-CONTRAST, Response time: Photodiode)

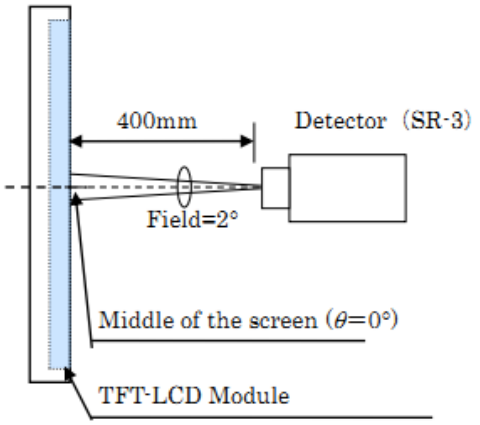


Fig.9-2 Measurement of Contrast, Luminance, Chromaticity, White variation, Crosstalk andColor temperature variation.

[Note 9-3]Definitions of viewing angle range

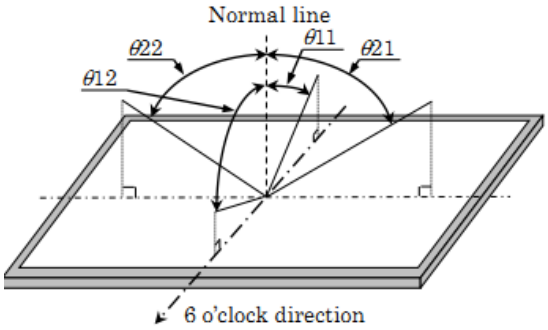


Fig.9-3 Viewing angle

[Note 9-4]Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio} = \frac{\text{Luminance(Brightness) with all pixels white}}{\text{Luminance(Brightness) with all pixels Black}}$$

[Note 9-5]Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

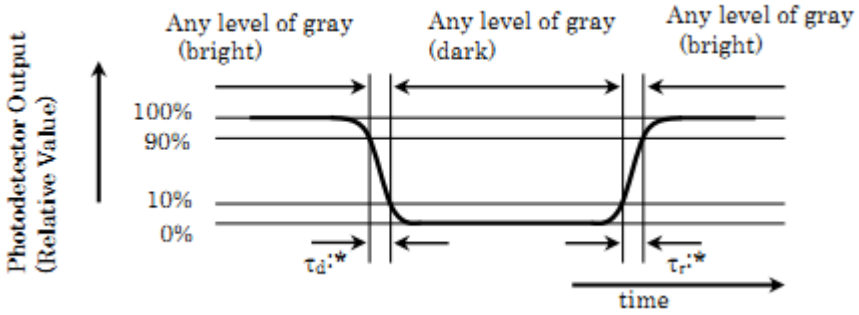
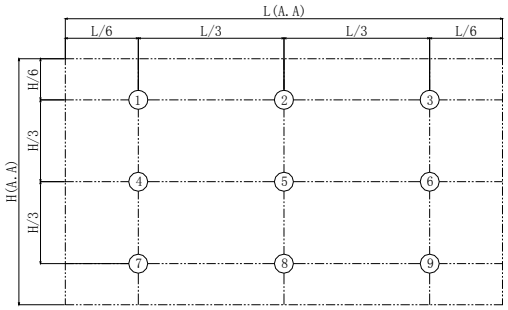


Fig.9-4 Response time

[Note 9-6] This shall be measured at center of the screen.



[Note 9-7]Definition of white uniformity:

White uniformity is defined as the following with 9 measurements

$$\delta W = \frac{\text{Minimum Luminance of 9 Points(Brightness)}}{\text{Maximum Luminance of 9 Points(Brightness)}}$$

10. Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

11. Handling Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
Please insert for too much stress not to join a connector in the case of insertion of a connector.

b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

c) Since the front polarizer is easily damaged, pay attention not to scratch it.

d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

g) Since CMOS LSI is used in this module, take care of static electricity and injure the human earth when handling. Observe all other precautionary requirements in handling components.

h) This module has its circuitry PCBs on the side and should be handled carefully in order not to be stressed.

i) Laminate film is attached to the module surface to prevent it from being scratched. Peel the laminate film off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc. Working under the following environments is desirable.
・All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without ail.
・Use Ionized blower for electrostatic removal, and peel of the laminate film with a constant speed. (Peeling of it at over 2 seconds)

j) The polarizer surface on the panel is treated with Anti-Glare. In case of attaching protective board over the LCD, be careful about the optical interface fringe etc. which degrades display quality.

k) Do not expose the LCD module to a direct sunlight, for a long period of time to protect the module from the ultra violet ray.

l) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive,resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.

m) Liquid crystal contained in the panel may leak if the LCD is broken. Rinse it as soon as possible if it gets inside your eye or mouth by mistake.

n) Disassembling the module can cause permanent damage and should be strictly avoided.
Please don't remove the fixed tape, insulating tape etc that was pasted on the original module.
(Except for protection film of the panel.)

o) Be careful when using it for long time with fixed pattern display as it may cause afterimage.
(Please use a screen saver etc., in order to avoid an afterimage.)

p) If a minute particle enters in the module and adheres to an optical material, it may cause display non-uniformity issue, etc. Therefore, fine-pitch filters have to be installed to cooling and inhalation hole if you intend to install a fan.

q) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.
Be sure to confirm the component of them.

r) Do not use polychloroprene. If you use it, there is some possibility of generating Cl2 gas that influences the reliability of the connection between LCD panel and driver IC.

s) Do not put a laminate film on LCD module, after peeling of the original one. If you put on it, it may cause discoloration or spots because of the occurrence of air gaps between the polarizer and the film.

t) Ground module bezel to stabilize against EMI and external noise.

12. Packaging Condition(TBD)

Piling number of cartons	
Package quantity in one carton	
Carton size	
Total mass of one carton filled with full modules	
Packing form	

13. Label (TBD)

1) Module Bar code label:

TBD

2) Packing bar code label

TBD

14. RoHS Directive

This LCD open-cell is compliant with RoHS Directive.

15. Reliability Test Items

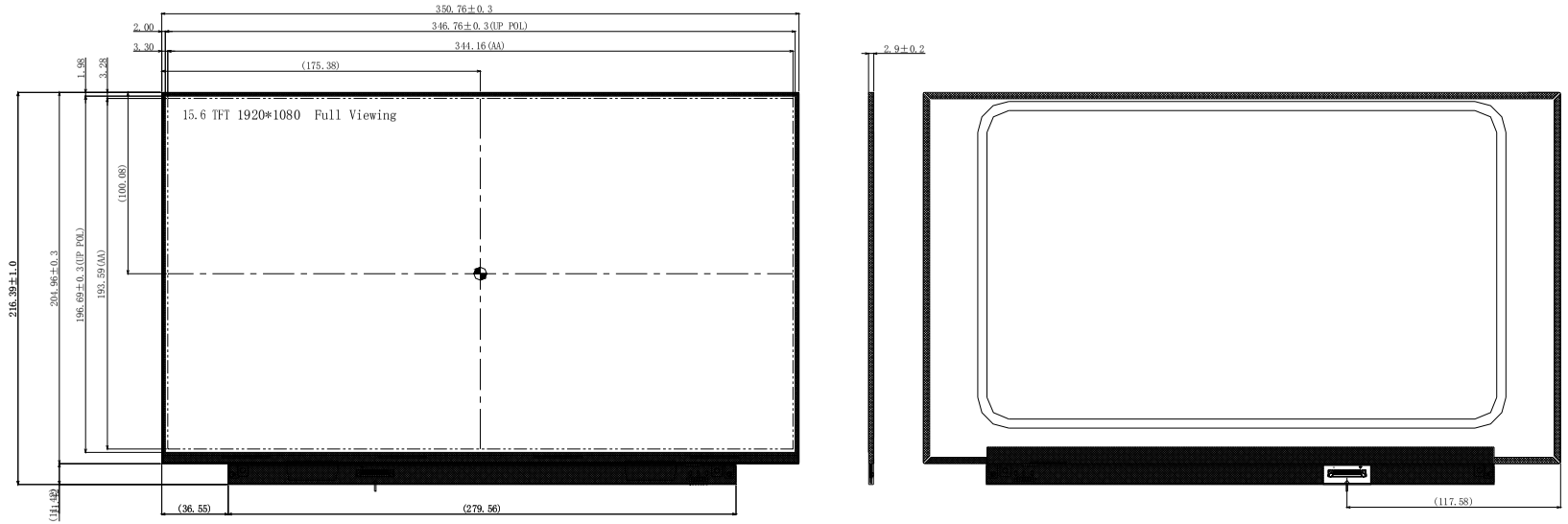
No.	Test Item	Conditions
1	High temperature storage test	Ta=60℃ 72h
2	Low temperature storage test	Ta=-20℃ 72h
3	High temperature & high humidity operation test	Ta=40℃90%RH 70h (No condensation)
4	High temperature operation test	Ta=50℃ 72h
5	Low temperature operation test	Ta=0℃ 72h

[Result Evaluation Criteria] Under the display quality test condition with normal operation state.

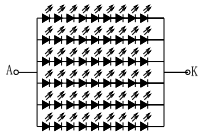
Do not change these condition as such changes may affect practical display function.

[Normal operation state] temperature：＋15~＋35℃，Humidity：45~75%，Atmospheric pressure：86~106kPa

				Customer Code.:		SPECIFICATION OF BACKLIGHT	
				CUSTOMER'S P/N:		EDITION:	01
Date:	2022.10.11	Page:	1/1	THE THIRD ANGLE	P/N(exclude wrapper):	P/N: (include wrapper)	
						Approval(核准)	
						Check (检查)	
						Design(设计)	



Notes:
1.Unit:mm.
2.Do not scale drawing.
3.All radii without dimension R0.2.
4. △Modification Mark.
5.draft angle: 1°
6.Center luminance :250d/m^2(Min)~280d/m^2(TYP)
7.Luminace uniformity: 75%(min)(min/max*100%)
8.UnSpecified Tolerance is ±0.2
9.Operation conditions :If= 120mA, Vf=27(TYP)
Color coordinate:X=TBD±0.05,Y=TBD±0.05
10.All materials comply with RoHS
11.The measured value of luminace and color coordinate bases SMT'S CA-210
12:Check item:1~9



Backlight LED 9串6并54颗 Circuit

NO.	TITLE	Quantity
12	Front iron frame (上铁框)	
11	FPC (软制电路板)	
10	Double_sided stick (双面胶)	
9	HOUSING (塑胶框)	
8	PCB(印制电路板)	
7	Wire (导线)	
6	LED(发光二极体)	
5	BEF(增光片)	
4	Diffuser film(扩散片)	
3	Light guide plate(导光板)	
2	Reflector film (反射膜)	
1	Rear iron frame (下铁框)	

REV	DATE	DESCRIPTION (修改内容)	REVISER

Customer: 客 户		Approval Date: 确认日期		Approve by: 确 认