



深圳市智诚光电发展有限公司

LCD MODULE

SPECIFICATION

Customer: _____
Model Name: ZC080IA05
Date: 2021/8/27
Version: 01

- Preliminary Specification
 Final Specification

Remark

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by
		

Preliminary Product Specification

保管單位 Storage	PM
保存年限 Retention Period	3年

REVISION STATUS

Revision	Description	Page	Revision Date
1	Preliminary Spec		2021-6



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A. General Specifications

(1) Overview

The ZC080IA05 is a 8-inch LCD Cell with thin film transistors as active elements and contains 1280x 720pixels. Each pixel is divided into red, green and blue dot, which are arrange in vertical stripe. The FOG is normally black mode, and can be applied to the transmission type display. Backlight unit (BLU) is not built in.

(2) General Specification

NO.	Item	Specification
1	Display resolution (pixel)	1280*RGB*720
2	Active area (mm)	177.024mm(V) * 99.576mm (H)
3	Screen size (inch)	8 inches diagona
4	Pixel pitc (mm)	0.1383mm x 0.1383mm
5	Outline Dimension (mm)	192.8MM*116.9MM*4.5MM
6	Weight (g)	TBD
7	Surface treatment	HC
8	Interface	LVDS
9	Shipment	MOD
10	Contrast ratio	1000
11	Response Time	25ms (typ) @ B/W
12	Transmittance	3.2% (Typ)

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B. Absolute Maximum Ratings

LCM					
Item	Symbol	Min	MAX	Unit	Remark
Power Supply Voltage 1	VDD	-0.3	3.96	V	
Power Supply Voltage 2	AVDDP	-0.3	6.5	V	
Power Supply Voltage 3	AVDDN	-6.5	0.3	V	
Power Supply Voltage 4	Vcom	-3	1	V	
Power Supply Voltage 5	VGH	17	21	V	Note1
Power Supply Voltage 6	VGL	-15	-11	V	Note1

Note1 : VGH、VGL在极值电压条件下，只能保障面板Function OK，无法保障面板RA504hrs高低温测试信赖性。

C. Pin Assignment

Connector Part No.: 40 Pin.(F31L-1A7H1-21040)

Pin N .	Symbol.	I/O.	Description	Note		
1	VGL	P	Power supply for analog power			
2	Dummy					
3	VGH	P	Power supply for analog power			
4	Dummy					
5	AVDDN	P	Power supply for analog power			
6	Dummy					
7	AVDDP	P	Power supply for analog power			
8	Dummy					
9	GND	P	Ground			
10	CSB	I	Serial Interface chip enable signal. CSB=0: Selected (accessible) CSB=1: Not selected (inaccessible)			
11	SCL	I	Serial Interface clock input.			
12	SDA	I/O	Serial Interface address and data input/output.			
13	TB	I	Vertical shift direction (gate output) selection.			
			TB		Function	Note
			1		Top→bottom	Default
0	Bottom→top	-				
14	RL	I	Horizontal shift direction (source output) selection.			
			RL		Source output sequence and data order	Note
			1		SOUT1→SOUT2→ ...→SOUT2400	Default
0	SOUT2400→SOUT2399→ ...→SOUT1	-				
15	DINT	I	Input data format selection.			

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			DINT	Function	Note
			1	8-bit	Default
			0	6-bit	-
16	BISTEN	I	Enable built-in self test (BIST) function.		
			BISTEN	Function	Note
			1	BIST mode	-
			0	Normal mode	Default
17	STBYB	I	Standby mode setting pin. The chip is in standby mode when STBYB=0.		
18	RESETB	I	Reset pin. The chip is in reset state when RESETB=0.		
19	GND	P	Ground		
20	LVD0N	I	LVDS Data Lane 0 Negative		
21	LVD0P	I	LVDS Data Lane 0 Positive		
22	GND	P	Ground		
23	LVD1N	I	LVDS Data Lane 1 Negative		
24	LVD1P	I	LVDS Data Lane 1 Positive		
25	GND	P	Ground		
26	LVCLKN	I	LVDS Clock Lane Negative		
27	LVCLKP	I	LVDS Clock Lane Positive		
28	GND	P	Ground		
29	LVD2N	I	LVDS Data Lane 2 Negative		
30	LVD2P	I	LVDS Data Lane 2 Positive		
31	GND	P	Ground		
32	LVD3N	I	LVDS Data Lane 3 Negative		
33	LVD3P	I	LVDS Data Lane 3 Positive		
34	GND	P	Ground		
35	Dummy				
36	VDD	P	Power supply for analog power		
37	Dummy				
38	VDDOTP		Customer must be floating		
39	Dummy				
40	Vcom	P	Power supply for analog power		

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D. Optical specifications

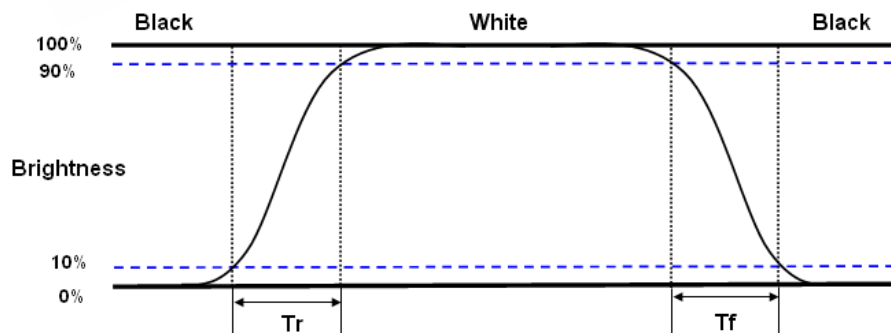
Item	Symbol	Condition	Specification			Unit	Remark
			Min.	Typ.	Max.		
Response time	Tr+Tf	$\theta = 0^\circ$	-	25	35	ms	Note 1
Contrast ratio	CR	$\theta = 0^\circ$	800	1000	-		Note 2
Viewing angle	Top	$CR \geq 10$	75	85	-	deg.	Note 3
	Bottom		75	85	-		
	Left		75	85	-		
	Right		75	85	-		
Color chromaticity (CF only with OC, light source is C light, CIE 1931)	Wx	$\theta = 0^\circ$	-0.015	0.306	+0.015	CIE	Note 4 Note 5
	Wy			0.328			
Color Gamut (CF only, Base on C Light)	NTSC	CIE1931	73	76	-	%	
Luminance	L	°	-	600	-		
Transmittance	Trans	$\theta = 0^\circ$	3.0	3.2	-	%	

Test Condition :

1. The ambient temperature is 25°C.
2. The test systems refer to Note 4.

Note 1: Definition of response time:

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time is the time between photo detector output intensity changed from 10% to 90%. And fall time is the time between photo detector output intensity changed from 90% to 10%.



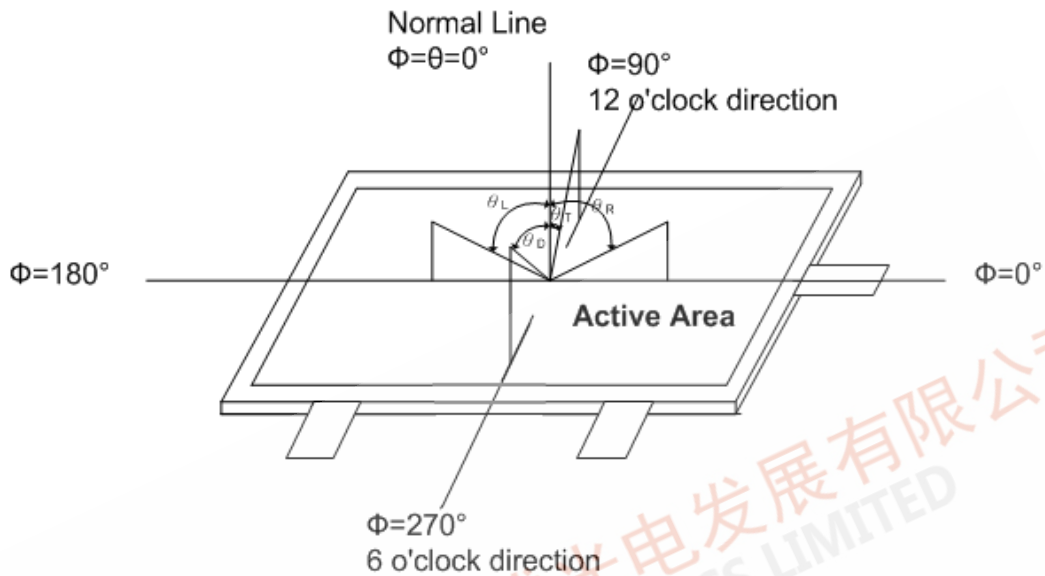
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Note 2: Definition of contrast ratio:

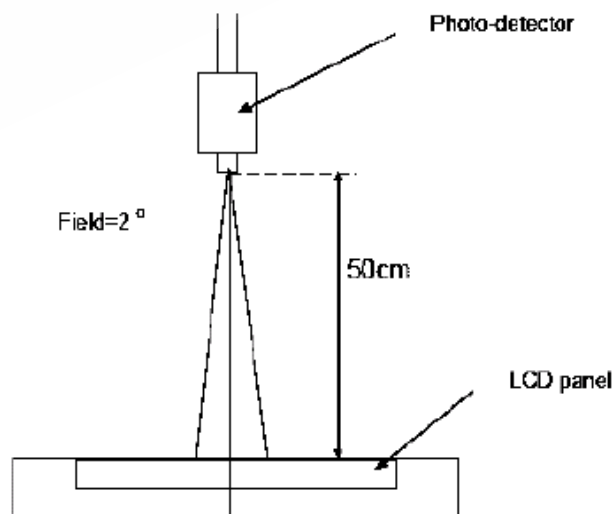
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 3: Definition of viewing angle



Note 4: Optical characteristic measurement setup.

The LCD module should be stabilized at given temperature for 10 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 10 minutes in a windless room.



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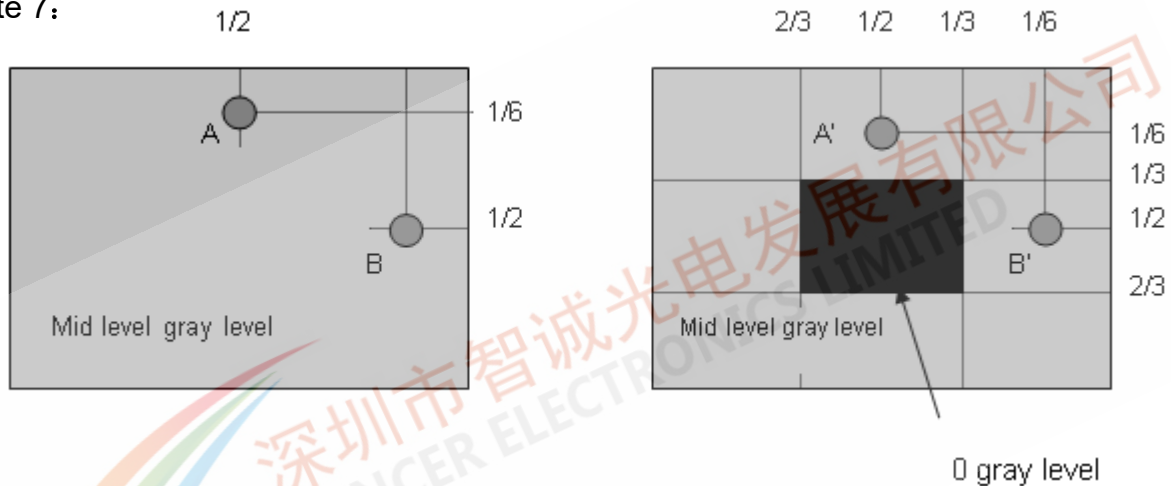
Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note 6: Measuring Conditions:

The optical characteristics are determined after the unit has been 'ON' and stable at the maximum brightness, in a dark environment at an ambient temperature at $25^{\circ}\text{C} \pm 2^{\circ}\text{C}$. The electrical conditions include $V_{cc} = 3.3\text{ V}$, $f_v = 60\text{ Hz}$. Recommended measuring equipments for luminance and color is BM5A Colorimeter with a viewing cone of 2° or similar. The measuring distance should be about 30-50 cm from the LCD surface at normal unless otherwise specified. The (virtual) measuring spot should be 5mm in diameter. The CIE 1931 Standards shall be used. Viewing angle measurements should be done by the CS2000 EZ Color system or similar.

Note 7:



Unit: percentage of dimension of display area

$|L_A - L_{A'}| / L_A \times 100\% = 2\% \text{ max.}$, L_A and $L_{A'}$ are brightness at location A and A'

$|L_B - L_{B'}| / L_B \times 100\% = 2\% \text{ max.}$, L_B and $L_{B'}$ are brightness at location B and B'

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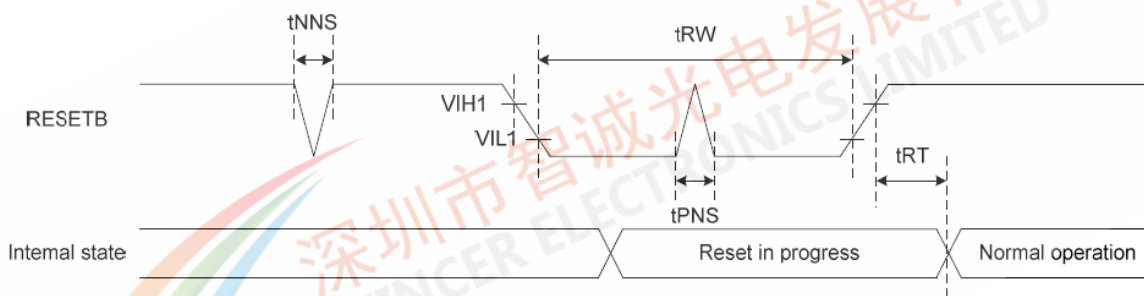
E. Electronic Specification

(1). Typical Operation Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit	Remark
Analog Operating voltage	VDD	2.8	3.3	3.6	V	
Analog Operating voltage	AVDDP	5	5.5	6	V	
Analog Operating voltage	AVDDN	-6	-5.5	-5	V	
Analog Operating voltage	Vcom	-2	-1	0	V	Note1
Analog Operating voltage	VGH	18	19	20	V	
Analog Operating voltage	VGL	-14	-13	-12	V	

Note1 : 由客户系统端提供最适 Vcom.

(2). Reset timing



(VDD=2.7 to 3.6V, GND=0V, TA=-40 to +95°C)

Signal	Paramete	Symbol	Spec.			Unit	Remarks
			Min.	Typ.	Max.		
RESETB	Reset pulse width	tRW	10	-	-	us	-
	Reset complete time	tRT	-	-	5	us	-
	Positive spike noise width	tPNS	-	-	100	ns	-
	Negative spike noise width	tNNS	-	-	100	ns	-

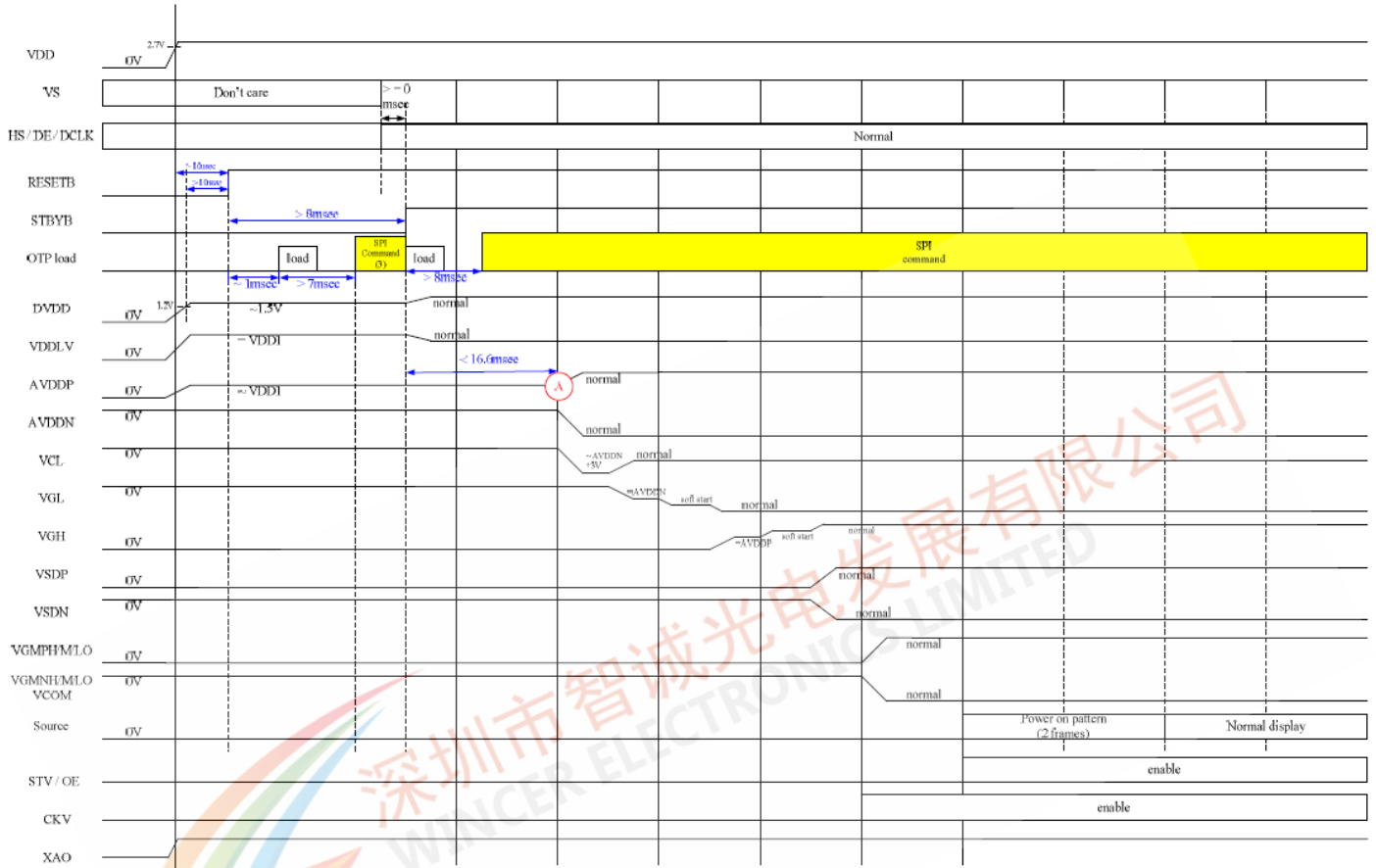
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(3). Power on / off Sequence

Power on sequence

External power AVDDP/AVDDN need to be supplied before point A

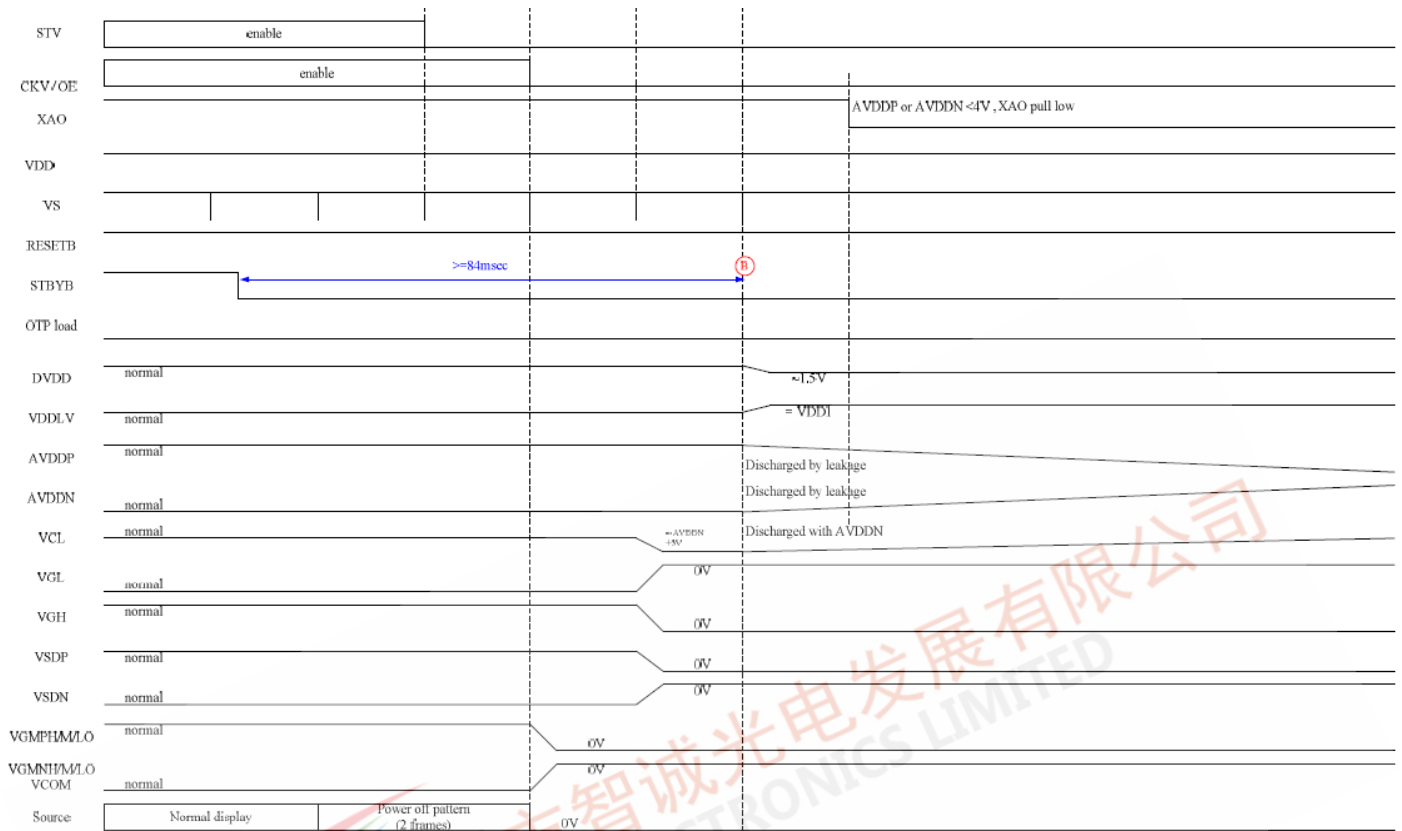


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Power off sequence

External power AVDDP/AVDDN need to be removed after point B

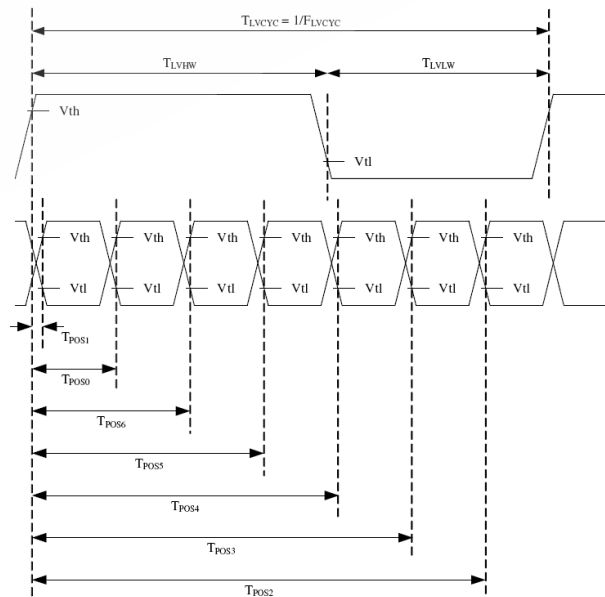


(4). Timing Characteristics

LVDS input timing is described as below.

LVCLKP(R)-LVCLKN(R)

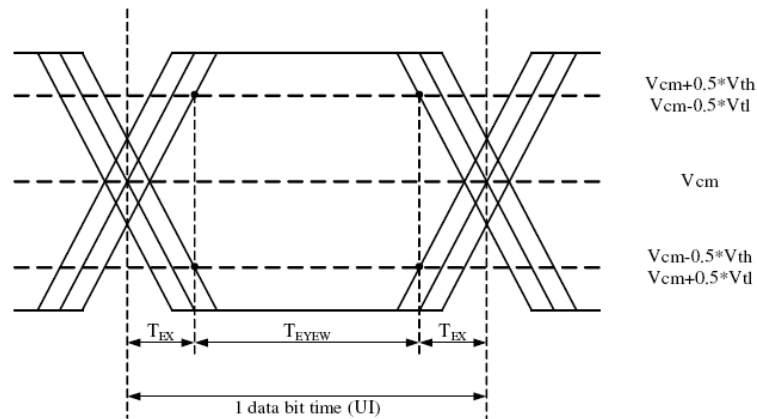
LVD[3:0]P(R)-
LVD[3:0]N(R)



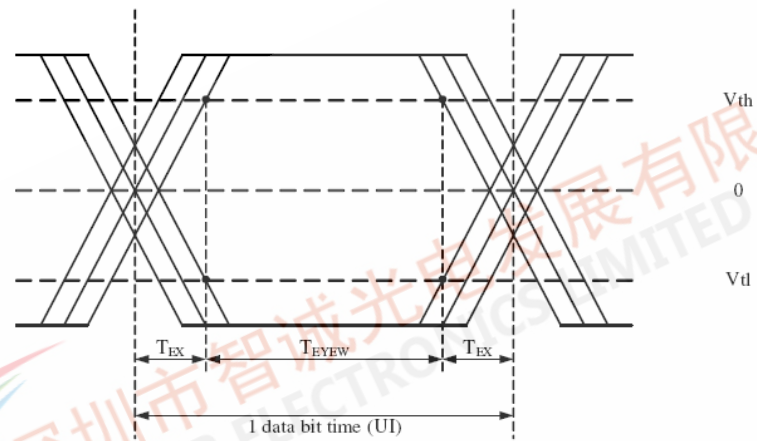
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Single-ended:LVD[3:0]P,LVD[3:0]N



Differential:LVD[3:0]P-LVD[3:0]N



Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency	FLVCYC	10	-	85	MHz
Clock period	TLVCYC	11.76	-	100	nsec
1 data bit time	UI	-	1/7	-	TLVCYC
Position 1	TPOS1	-0.2	0	0.2	UI
Position 0	TPOS0	0.8	1	1.2	UI
Position 6	TPOS6	1.8	2	2.2	UI
Position 5	TPOS5	2.8	3	3.2	UI
Position 4	TPOS4	3.8	4	4.2	UI
Position 3	TPOS3	4.8	5	5.2	UI
Position 2	TPOS2	5.8	6	6.2	UI
Input eye width	TEYEW	0.6	-	-	UI
Input eye border	TEX	-	-	0.2	UI
LVDS wake up time	TENLVD S	-	-	150	μ s

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LVDS with SSC

The LVDS receiver can support spread spectrum clock (SSC). Limitation is listed as below. Note that modulation frequency is proportional to LVDS clock frequency.

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Modulation Frequency	SSC _{MF}	-	-	200	Khz	LVDS clock frequency centered at 80MHz.
		-	-	150	Khz	LVDS clock frequency centered at 60MHz.
		-	-	100	Khz	LVDS clock frequency centered at 40MHz.
		-	-	50	Khz	LVDS clock frequency centered at 20MHz.
Modulation Rate	SSC _{MR}	-	-	±5	%	LVDS clock frequency + SSC _{MR} is in the range of 10~85MHz.

Porch setting (LVDS: VESA format, VS/HS Polarity: Low active)

Parameter	Symbol	Panel Resolution		
		1280 x RGB x 720 RS[3:0]=Ah		
		Min.	Typ.	Max.
DCLK Frequency	FDCLK	58.5	63.7	76.3
Horizontal valid data	thd	1280		
Hsync Pulse Width	thpw	1	2	172
Hsync back porch	thbp	5	16	173
Hsync front porch	thfp	16	44	187
1 Horizontal Line	th	1336	1340	1472
Vertical valid data	tvd	720		
Vsync Pulse Width	tpw	1	2	138
Vsync back porch	tvbp	5	5	139
Vsync front porch	tvfp	5	67	139
1 Vertical field	tv	730	792	864

Note: (1) DCLK Frequency min/max value is base on frame rate 60 Hz.

Note: (2) thbp+thpw+thfp >=56 DCLK, tvbp+tpw+tvfp>=10.

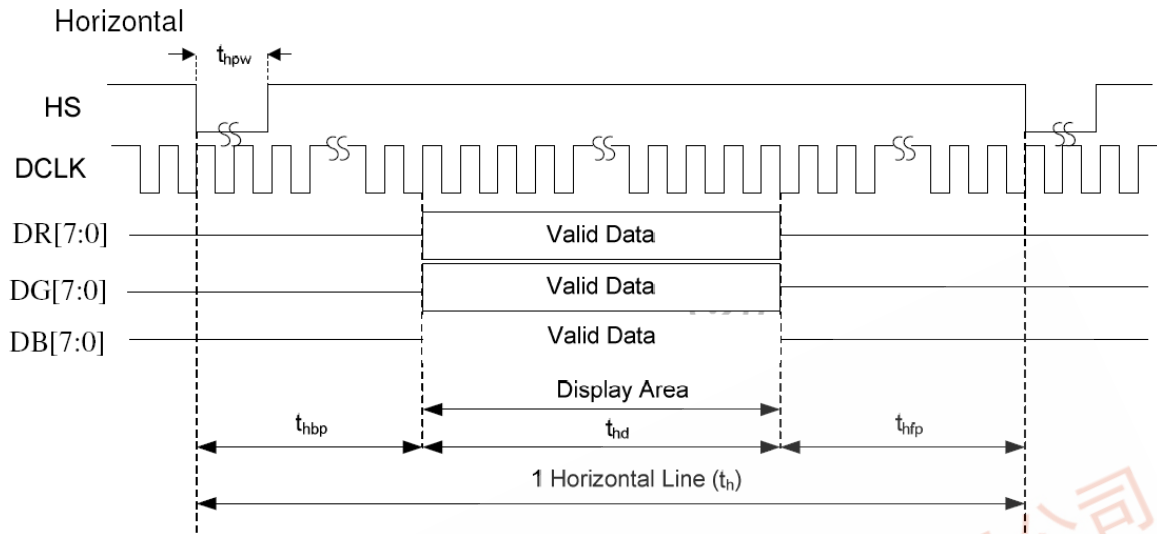
Note: (3) back porch value include pulse width value

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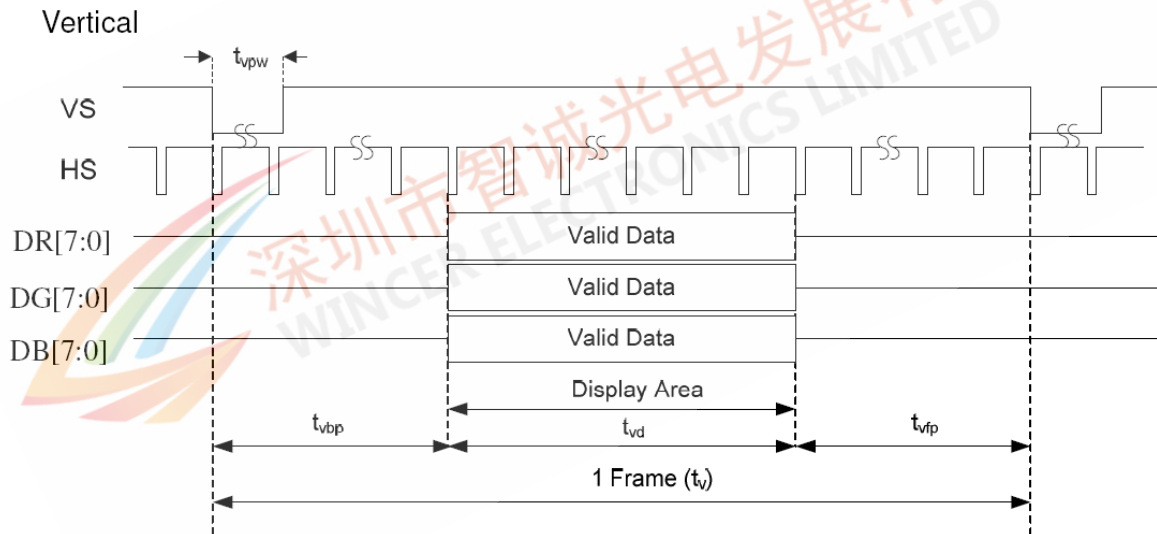
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Parallel RGB at Sync mode Drawing

Horizontal input timing at Sync mode



Vertical input timing at Sync mode



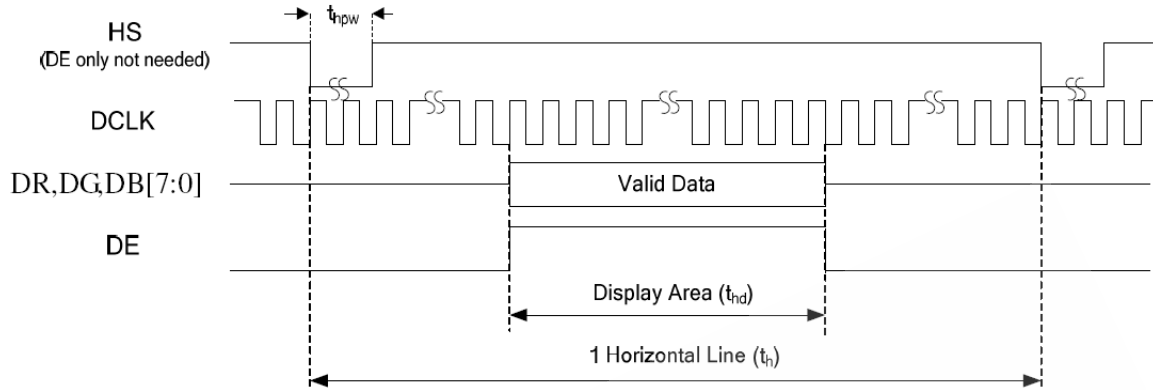
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Parallel RGB at DE mode Drawing

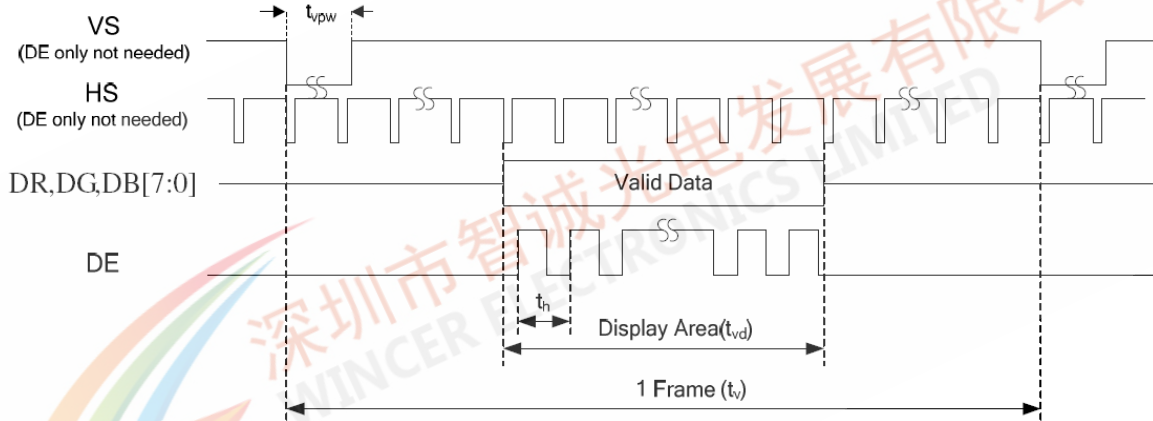
Horizontal input timing at DE only mode

• Horizontal



Vertical input timing at DE only mode

• Vertical



Parameter	Symbol	Panel Resolution		
		1280 x RGB x 720		
		Min.	Typ.	Max.
DCLK Frequency	FDCLK	58.5	63.7	76.3
Horizontal valid data	thd	1280		
1 Horizontal Line	th	1336	1340	1472
Vertical valid data	tvd	720		
1 Vertical field	tv	730	792	864

Note: (1) DCLK Frequency min/max value is base on frame rate 60 Hz.

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F. Reliability Assurance Specification

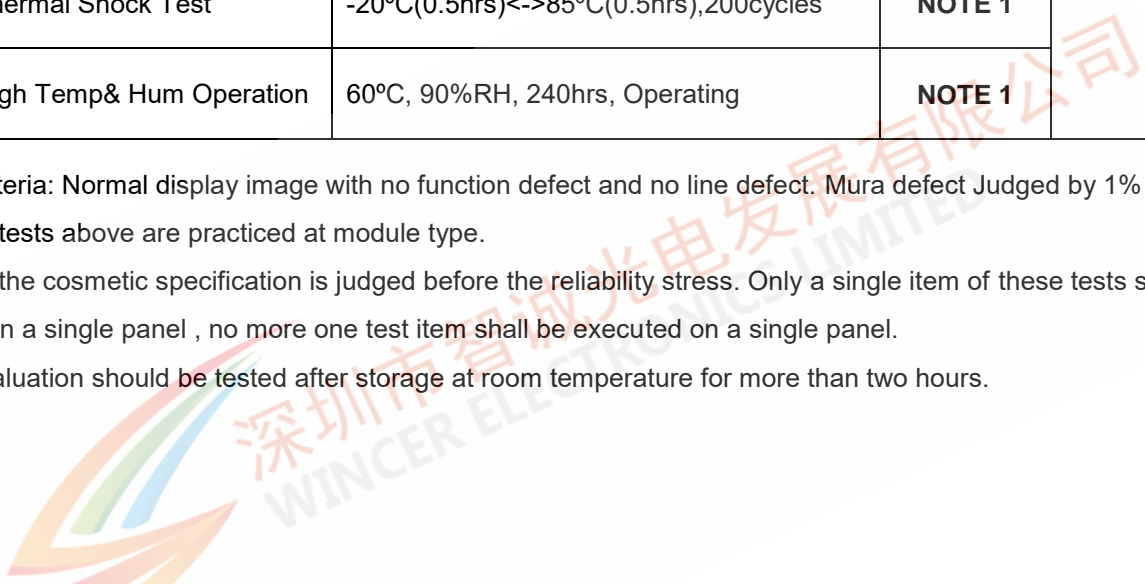
Test Item	Test Condition	Judgment	Remark
High Temp. Storage	85°C, 240hrs,Storage	NOTE 1	NOTE 2 NOTE 3 NOTE 4
Low Temperature Storage	-30°C, 240hrs,Storage	NOTE 1	
High Temp. Operation	85°C,240hrs,Operating	NOTE 1	
Low Temperature Operation	-20°C, 240hrs,Operating	NOTE 1	
Thermal Shock Test	-20°C(0.5hrs)<->85°C(0.5hrs),200cycles	NOTE 1	
High Temp& Hum Operation	60°C, 90%RH, 240hrs, Operating	NOTE 1	

Note1: Criteria: Normal display image with no function defect and no line defect. Mura defect Judged by 1% ND filter

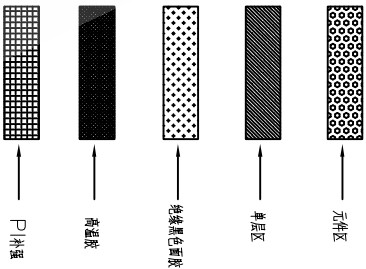
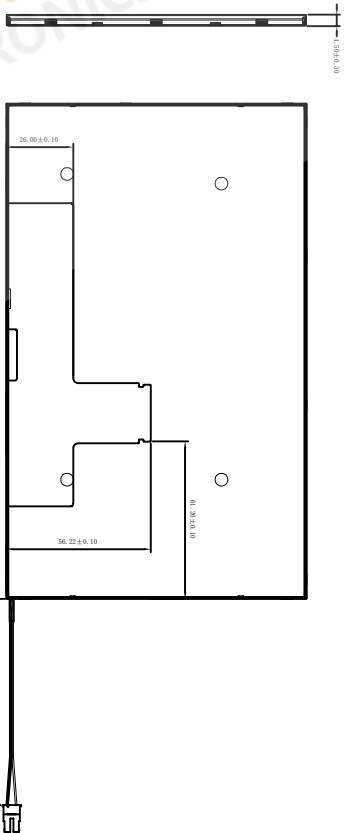
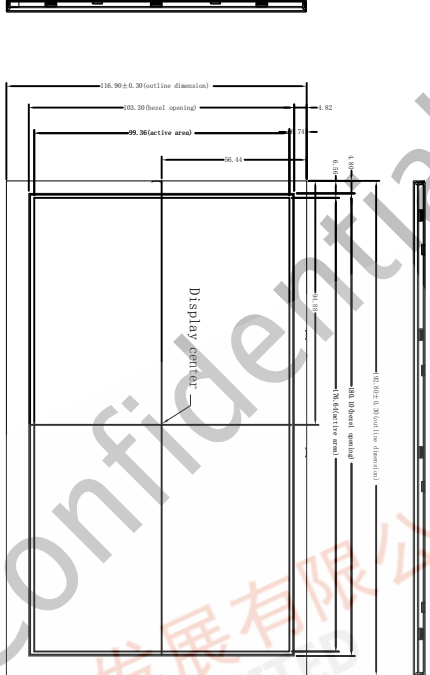
Note2: All tests above are practiced at module type.

Note3: All the cosmetic specification is judged before the reliability stress. Only a single item of these tests shall be executed on a single panel , no more one test item shall be executed on a single panel.

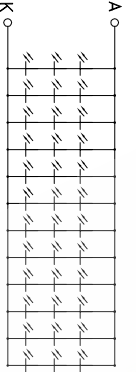
Note4: Evaluation should be tested after storage at room temperature for more than two hours.



MARK	REVISER	DATE	REVISED DESCRIPTIONS



CIRCUIT DIAGRAM (LED 3*12=36 DISE)



ELECTRICAL-OPTICAL CHARACTERISTICS
(To=25°C. The Ambient temperature To=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Forward Current	I _f	I _f = 360 mA	8.7	9.6	10.2	V
Reverse Current	I _r	V _r = 5 V				μA
Power dissipation	P _d	I _f = 360 mA		0.31		W
Colour Coordinates	x, y	I _f = 360 mA		0.33		
Bl. luminance (Center Area)	L _v	I _f = 360 mA	/	/	/	cd/m ²
Luminous Uniformity (Center)	L _v	I _f = 360 mA	75			%
LCM Luminance	L _v	I _f = 360 mA		800		cd/m ²
Operating Temperature Range	T _{op}	normal use	-20		+70	°C
Storage Temperature Range	T _{stg}	normal use	-30		+80	°C

REV	REV	MODEL NAME	UNIT	mm	APPROVED	CHECKED	DRAWN BY
A0	AO	标题 型号	单件	mm	核准	检查	绘图
SCALE	TITLE	UNMARKED TOLERANCE	DATE	2020.09.09			
1:1	名称	日期					